

# An Efficient Implementation of Random Walking Coding For Communication Channels

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**Abstract** - The problem of simultaneously broadcasting a common source to multiple receivers over a broadcast channel remains a challenging open problem in network information theory. Each receiver is required to partially reconstruct the source sequence by decoding a certain fraction of the source symbols. Our scheme involves splitting the source sequence into multiple segments and applying a systematic erasure code to each such segment. A new Randomized Tree Walking Algorithm, which is secure against active eavesdroppers and allows for the efficient interrogation of many channels. In order to reduce a data flipping in encoder and decoder a novel encoding method is also proposed for communication. Our proposed architecture has been coded in Verilog HDL and simulated using xilinx 12.1.

## I INTRODUCTION

CMOS VLSI is intrinsically a low-power technology. When compared to TTL, ECL or GaAs at similar levels of integration the power dissipated by CMOS is several orders of magnitude lower[1]. Nowadays, power dissipation is a very burning topic, everybody in search of how to minimize power dissipation in daily use devices like laptops, mobile phones, mp3 players etc[6]. The dynamic power dissipated by a CMOS circuit is of the form [1]:

$$P_{chip} \propto \sum_{i=1}^N C_{load_i} \cdot V_{dd}^2 \cdot f \cdot p_i$$

where the sum is done over all the  $N$  nodes of the circuit,  $C_{load_i}$  is the load capacitance at node  $i$ ,  $V_{dd}$  is the power supply voltage,  $f$  is the frequency and  $p_i$  is the activity factor at node  $i$ .

As the number of cores integrated into a system on chip (SoC) increases, the role played by the interconnection system becomes more and more important[2]. Thus, the design of Systems-on-Chip (SoCs) is usually based on the reuse of predesigned and pre-verified intellectual property core that are interconnected through special communication resources that must handle very tight of performance

and area constraints[3]. Sophisticated power-aware, high-level language compilers, dynamic power management policies, memory management, bus-encoding techniques, and hardware design tools are demanded to meet these often-conflicting design requirements. This paper focuses on the low power bus-encoding problem[7]. Managing the power of an Integrated Circuit (IC) design has become a major concern of IC designers. In this paper, we focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales.

Most of the previous bus-encoding schemes were designed to minimize transition activities on each signal line as if each line were isolated from neighboring lines, hence ignoring coupling effects. Such an assumption may be valid for off-chip buses where the impedances of transmission lines are appropriately adjusted[8]. A novel intra cache-block spatial locality predictor, to identify words unlikely to be used before the block is evicted. A static packet encoding technique which leverages spatial locality prediction to reduce the network activity factor, and hence dynamic energy, in the NoC routers and links. The static encoding requires no modification to the NoC and minimal additions to the processor caches to achieve significant energy savings with negligible performance overhead. A complementary dynamic packet encoding technique which facilitates additional energy savings in transmitted its, reducing switching activity in NoC links and routers via light-weight microarchitectural support[10].

The basic elements which form a NoC-based interconnect are network interfaces (NIs), routers, and links. As technology shrinks, the power dissipated by the links is as relevant as (or more relevant than) that dissipated by routers and NIs. In this paper we focus on power dissipated by network links. Links dissipate power due to the switching activity (both self and coupling) induced by subsequent data patterns traversing the link [2]. Data compression is an efficient method to decrease power dissipation and by removing the extra redundancy the data can be accurately

approximated as a random sequence. Even if compression is not used we believe that a random process is a reasonable approximation for the sequence on a data bus for our purpose [1]. We focus on data encoding schemes as a viable way to reduce power dissipated by the network links. The basic idea is to opportunely encode the data before their injection in the network in such a way as to reduce the switching activity of the links by using the clock gating techniques.

The rest of this brief introduces the scheme by first summarizing data encoding and the related works are considered in Section II. Then, in Section III, the proposed scheme is presented. Section IV and V presents a experimental Results and performance analysis to illustrate the effectiveness of the approach. Finally, the conclusions are summarized in Section VI.

## II RELATED WORKS

Successive Segmentation-based Coding for Broadcasting over Erasure Channels. Motivated by error correction coding in multimedia applications, we study the problem of broadcasting a single common source to multiple receivers over heterogeneous erasure channels. Each receiver is required to partially reconstruct the source sequence by decoding a certain fraction of the source symbols. We propose a coding scheme that requires only off-the-shelf erasure codes and can be easily adapted as users join and leave the network. Our scheme involves splitting the source sequence into multiple segments and applying a systematic erasure code to each such segment. We formulate the problem of minimizing the transmission latency at the server as a linear programming problem and explicitly characterize an optimal choice for the code-rates and segment sizes. Through numerical comparisons, we demonstrate that our proposed scheme outperforms both separation-based coding schemes, and degree optimized rateless codes and performs close to a natural outer (lower) bound in certain cases. We further study individual user decoding delays for various orderings of segments in our scheme.

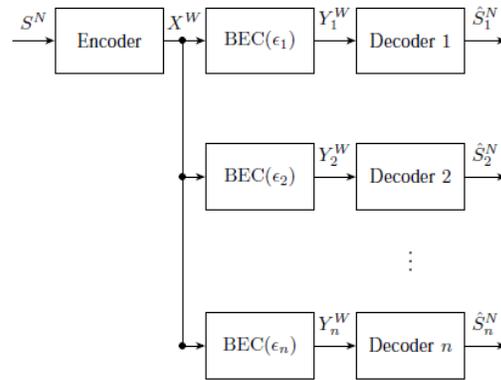


Fig. 1: Broadcasting an equiprobable binary source over an erasure broadcast channel.

we propose a coding scheme for transmitting to multiple receivers with heterogeneous channels and demands. Our scheme relies only on off-the-shelf erasure codes. The key idea in our scheme is to partition the source sequence into multiple non-overlapping segments and to apply a systematic erasure code to each segment. We formulate the problem of selecting the segment lengths and code rates that minimize the transmission latency as a linear programming problem and characterize an explicit solution. We discuss how the solution naturally evolves as users join or leave the network. We further compare our scheme numerically with separation-based schemes, and degree-optimized rateless codes and demonstrate that significant performance gains are possible. We also discuss how a tradeoff between the latencies of individual users can be attained by selecting various transmission orders for the parity checks.

Throughout this paper, we adhere to the notation defined herein. The sample space of a random variable is written in calligraphic font, e.g.,  $\mathcal{S}$ , and we let  $\mathcal{S}^N$  be the set of all  $N$ -vectors with components in  $\mathcal{S}$ . We use  $t$  when referring to the symbol index of a vector, which is enclosed in round brackets when actually referring to a vector component. Thus, the  $t$ th component of a vector  $\mathcal{S}^N$  is denoted by  $\mathcal{S}(t)$  so that  $\mathcal{S}^N$  in fact denotes  $(\mathcal{S}(1); \mathcal{S}(2); \dots; \mathcal{S}(N))$ . In general, a variable's subscript is reserved for user indices and indicates a correspondence between a user and the variable in question. For example, when the symbol  $d$  is used for distortion,  $d_i$  denotes the distortion of user  $i$ . Finally, for convenience, we also denote the set  $\{1; 2; \dots; N\}$  as  $[N]$ .

An "erasure" version of the symmetric problem was also studied, which considered an erasure distortion as well as a no-excess rate constraint for every  $m$  out of  $n$  descriptions. Interestingly, the coding scheme used built upon the ideas and resulted in a segmentation

based scheme similar to ours where the source was segmented into equal segments that were then each encoded with a systematic erasure code. In contrast, their work, however, did not involve any optimization over segment sizes. While these works do have high-level similarities and draw upon common practical motivations, there is another important distinction between our work and multiple description coding. This is that, fundamentally, the problem we consider is a joint-source channel coding problem. That is, in our formulation, the size of each channel symbol is fixed, while the number of channel uses approaches infinity. In contrast, in multiple description coding, the number of channels remains fixed, whereas the number of bits sent over each channel approaches infinity.

The segmentation-based code we present is also related to the coding scheme recently proposed, which was studied independently of our work and presented alongside it at a recent conference. In this work, the authors consider combining a successive refinement code with a timesharing strategy that individually channel codes messages intended for different users listening over the broadcast channel. As we will see, the code we present is similar in its use of a successive refinement code and a timesharing strategy. However, we will also see that our particular distortion measure is matched with the erasure channel in such a way that we are also able to benefit from the use of uncoded transmissions.

Finally, it is also worth mentioning that in terms of an outer bound, techniques that involve auxiliary channels have been developed for both the Gaussian model and a more general model of a discrete memoryless source sent over a discrete memoryless broadcast channel. While the techniques and inequalities used can be adapted for the erasure channel, we have found that doing so does not result in an outer bound that improves upon the point-to-point outer bound in the present setup. The difficulty encountered is in defining a suitable auxiliary channel that would lead to a non-trivial bound. Nevertheless, for a closely related problem involving the erasure broadcast channel and a Hamming distortion, non-trivial outer bounds can be obtained.

### III PROPOSED SYSTEM

The interconnection network dissipates a significant fraction of the total system power budget. For this reason, the design of power efficient interconnection networks is today recognized as a key issue. Several techniques have been proposed in the literature to reduce the power dissipated by the links of a NoC.

In this subsection, we review the sub-set of them which use data encoding schemes as main mechanism to reduce power dissipation[2].

The data encoding schemes we present in this paper have been already introduced by the authors in [12]. In this paper, the proposed schemes are discussed in more details and assessed by means of both a quantitative analysis and an experimental analysis.

The data encoding techniques may be classified into two categories. In the first category, encoding techniques concentrate on lowering the power due to self-switching activity of individual bus lines while ignoring the power dissipation owing to their coupling switching activity. In this category, bus invert (BI) and INC-XOR have been proposed for the case that random data patterns are transmitted via these lines. On the other hand, gray code, working-zone encoding, and T0-XOR were suggested for the case of correlated data patterns. Application-specific approaches have also been proposed.

The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity and the coupling switching activity in the links traversed by the flits. In fact, self-switching activity and coupling switching activity are responsible for link power dissipation. In this paper, we refer to the end-to-end scheme. The scheme presented is dealt with reducing the coupling switching. In this method, a complex encoder counts the number of Type I (Table I) transitions with a weighting coefficient of one and the number of Type II transitions with the weighting coefficient of two.

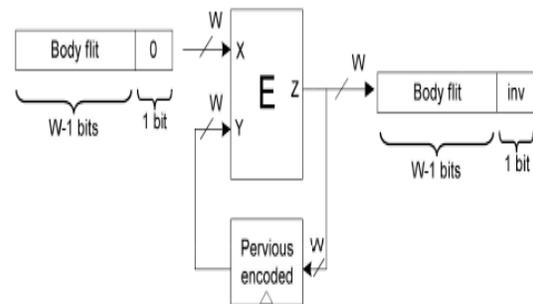


Fig. 2: Block diagram of encoding schemes

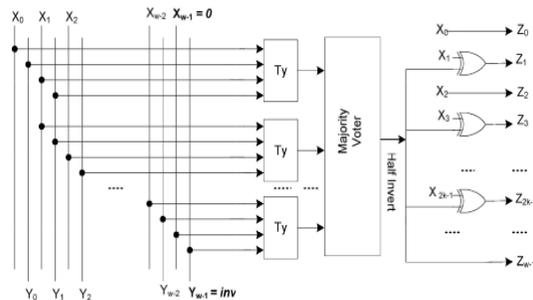


Fig. 3: Encoding scheme I

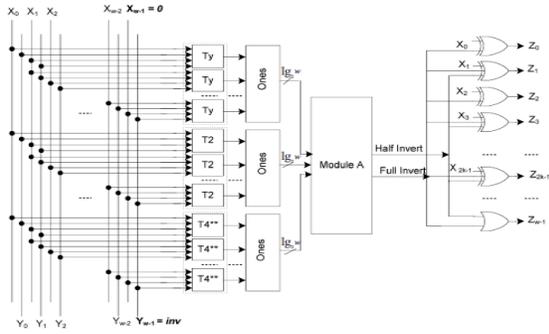


Fig. 4: Encoding scheme II

The authors in [12] considers a link width of  $w$  bits. The generic block diagram shown in Fig. 2 is the same for all three encoding schemes proposed in this paper and only the block E is different for the schemes. To make the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose  $w$  bits are the concatenation of  $w - 1$  payload bits and a “0” bit, represents the first input of the encoder, while the previous encoded flit represents the second input of the encoder which is based on the odd invert condition [Fig. 3]. The  $w - 1$  bits of the incoming (previous encoded) body flit are indicated by

s.no	Parameter	Existing	Proposed
1	TIME	6.62	6.52

$X_i (Y_i)$ ,  $i = 0, 1, \dots, w - 2$ . The  $w$  th bit of the previously encoded body flit is indicated by  $inv$  which shows if it was inverted ( $inv = 1$ ) or left as it was ( $inv = 0$ ). In the encoding logic, each  $T_y$  block takes the two adjacent bits of the input flits (e.g.,  $X_1X_2Y_1Y_2$ ,  $X_2X_3Y_2Y_3$ ,  $X_3X_4Y_3Y_4$ , etc.) and sets its output to “1” if any of the transition types of  $T_y$  is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation (Table I). The  $T_y$  block may be implemented using a simple circuit. The second stage of the encoder, which is a majority voter block, determines if the condition given in  $T_y > (w - 1)/2$  is satisfied (a higher number of 1s in the input of the block compared to 0s). If this condition is satisfied, in the last stage, the inversion is performed on odd bits. The decoder circuit simply inverts the received flit when the inversion bit is high.

Similar in Fig.3, In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts

Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction, where the Types were proposed in [14]. Here 1s blocks which count the number of 1s in their inputs. The output of these blocks has the width of  $\log_2 w$ . The output of the top 1s block determines the number of transitions that odd inverting of pair bits leads to the link power reduction. The middle 1s block identifies the number of transitions whose full inverting of pair bits leads to the link power reduction. Finally, the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power. Based on the number of 1s for each transition type, Module A decides if an odd invert or full invert action should be performed for the power reduction. The proposed encoding schemes using clock gating are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the NI. The encoders implementing the proposed schemes using clock gating have been assessed in terms of power dissipation and silicon area.

#### IV EXPERIMENTAL RESULTS

The proposed circuit are simulated and synthesized by using modelsim and xilinx12.1 which occurs low area than the existing. The experimental results are given in Table 1 and the simulation results of layout and the waveforms are shown in the fig.5 and fig.6. Then the RTL schematic of the proposed are shown in fig.6.

Table.1 comparison table

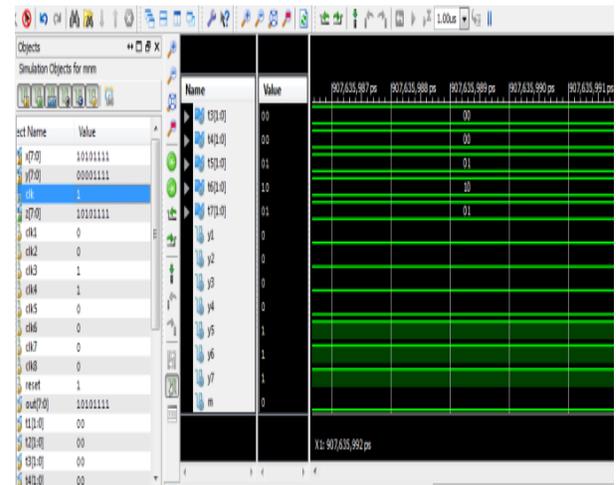


Fig. 5: simulation results

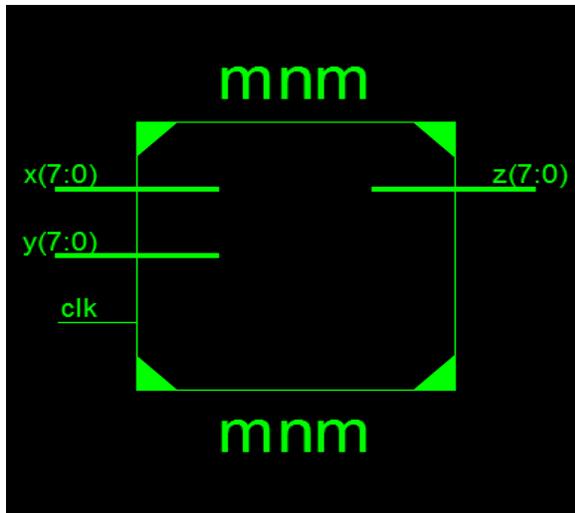


Fig. 6: RTL schematic

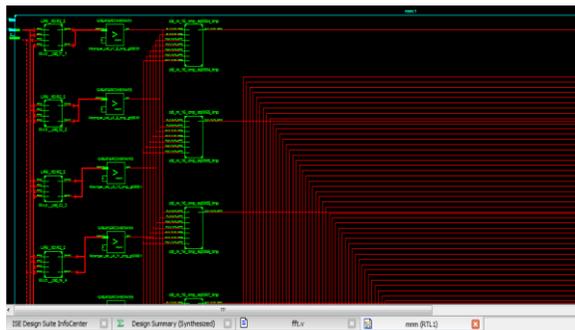


Fig 7: gatelevelnetlist

## V PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction in time and area based on the implementation results which have been done by using Spartan-3 processor.

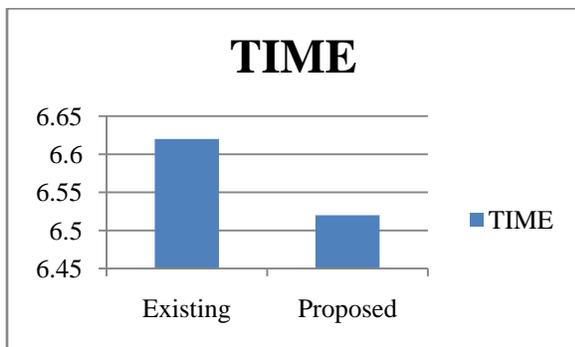


Fig. 8: performance analysis of existing and proposed

## VI CONCLUSION

In this project, we proposed a successive segmentation-based minimum switching activity coding scheme for broadcasting a binary source over a multi receiver erasure broadcast channel. Each receiver has individual distortion constraints and experiences distinct channel erasure rates. The relatively high switching energy is one of the major weaknesses of emerging communication. Accordingly, bit change reduction schemes are a particularly successful approach to reduce the impact of this overhead through the minimization of the number of bits changed per transmission. The proposed scheme partitions the source sequence into multiple segments and applies a systematic erasure code to each segment. We provided optimal choices for segment sizes and code rates for each segment, which were based on the users' channel erasure rates, and distortion constraints.

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