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Original Article

Thermal-First Evaluation of SiC MOSFET and Si IGBT in a Bidirectional Non-Isolated Half-Bridge DC–DC Converter

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Abstract *- Thermal limits—not efficiency alone—ultimately define how much power a bidirectional DC–DC converter can safely handle. This paper takes a thermal-first look at a non-isolated half-bridge built with a SiC MOSFET (SCT50N120) and a Si IGBT (IKY150N65EH7) at 25˚. Instead of summing probe losses, total loss is reconciled from port powers and measures how much of it actually loads the heatsink through a sink-share factor β. From the measured sink and junction temperatures, an estimation of the physical sink-to-ambient resistance $R_{\theta sa}^{phys}$ and the hot-junction loss share α .A single $R_{\theta sa}^{phys}$ per hardware family explains both buck and boost with near-zero error: 0.63K/W for the MOSFET rig and 0.43K/W for the IGBT rig. Normalized results rank thermal severity by junction rise per kilowatt: MOSFET boost 55.6 (worst), MOSFET buck 45.6, IGBT boost 2.12, and IGBT buck 0.73. With $T_{j,target} = 110$, MOSFET boost has the smallest extra-loss headroom ($\approx 5.6W$), while IGBT buck has the largest ($\approx 1.66kW$); none of the cases reached device limits within 600s. The findings identify reverse power flow as the SiC bottleneck and point to practical fixes: reduce $R_{\theta cs}$ and $R_{\theta sa}$, tune dead time, and use synchronous freewheeling to cut diode and switching stress.*

Keywords *- Thermal Analysis, Junction Temperature, Sink-to-Ambient Thermal Resistance, Bidirectional DC–DC Converter, SiC MOSFET, IGBT, Port-Power Reconciliation, Normalized Thermal Metric.*

1. Introduction

Bidirectional DC–DC converters (BDCs) are central to modern electric drivetrains and DC energy networks. They move power in both directions between sources and storage, supporting traction and regenerative braking in EVs, smoothing batteries in microgrids, and stabilizing DC buses in renewable systems [1-3]. Among available topologies, the non-isolated half-bridge (buck–boost) is widely favored: it shares a common ground, needs relatively few parts, and is straightforward to control, so it appears frequently in battery-to-battery stages, on-board chargers, and distributed DC front-ends [4-6].

While efficiency matters, the real ceiling on power density and durability is thermal. Junction temperature limits ultimately dictate how hard devices can be pushed before heatsinks, airflow, and packaging dominate the design. Technology choice shifts this balance: silicon IGBTs handle high current well with low conduction loss and robust SOA, but their slower switching raises energy loss at higher frequencies; SiC MOSFETs switch faster, incur lower per-event energy, and allow higher permissible junction temperatures—provided heat can be removed effectively [4,7,8]. Recent reviews across BDCs for EVs and storage echo these trade-offs and consistently flag thermal design as the underlying constraint [1, 3, 5, 7- 9].

Bidirectional DC–DC converters have been widely studied for electric vehicles, energy storage systems, and DC microgrids. Recent reviews summarize the evolution of non-isolated BDC topologies, control methods, and typical operating ranges for traction and stationary applications [1–3,5,8–10]. These works highlight the half-bridge buck–boost structure as a popular choice because of its common ground, moderate device count, and compatibility with standard control schemes. They also emphasize that aggressive power-density targets make thermal design increasingly critical.

Several authors have compared SiC and Si devices in BDCs and related converter stages. For example, studies such as [4,11] report that SiC devices can reduce switching losses and enable higher switching frequencies, while IGBTs can remain attractive at high current levels because of their conduction characteristics and mature packaging. However, these comparisons are typically framed in terms of efficiency

or individual device waveforms and do not provide a converter-level thermal framework that separates the source, path, and sink of the generated heat.

In parallel, there is a substantial body of work on thermal management of power electronic converters in EV and storage applications [7]. These studies discuss cooling technologies, thermal interface materials, and heatsink design, and they often rely on datasheet thermal impedances combined with simplified lumped-parameter models. While effective for sizing, such approaches rarely incorporate measurement-based sink-share information or normalized thermal metrics that allow direct comparison between different device families and operating points.

Earlier studies on bidirectional converter thermal behavior, including our own prior work on basic BDC topologies [12], mainly focus on particular configurations and use conventional definitions of loss and thermal resistance. What remains missing is a measurement-based, thermal-first comparison of SiC MOSFET and Si IGBT legs in a non-isolated half-bridge BDC, where total loss is defined at the ports, the heatsink inflow is measured explicitly, and normalized metrics such as headroom to a target are used to rank thermal severity across modes and technologies.

Why current comparisons fall short, **e**xisting comparisons between SiC MOSFETs and Si IGBTs in bidirectional DC–DC converters generally emphasize efficiency and device-level loss breakdown, but they rarely treat thermal behavior as the primary design constraint. Most works either sum a limited set of probe-based losses or report heatsink and case temperatures without clearly separating (i) how much of the total converter loss actually reaches the heatsink and (ii) how effectively the cooling hardware rejects that heat [1–3,4,7–12].

This leads to two main issues: double-counting of losses when electrical probes are added on top of heatsink inflow, and a lack of a clean link between total processed power, thermal bottlenecks, and design margins. As a result, it is difficult to compare different device technologies fairly or to translate measured temperatures into actionable cooling requirements.

1.1. Research Gap and Problem Statement

There is therefore a need for a thermal-first evaluation framework that (i) defines total loss consistently at the converter ports, (ii) measures how much of that loss truly loads the heatsink, and (iii) links heatsink and junction temperatures to normalized metrics that are independent of the specific bus voltage and switching frequency. In particular, for a widely used non-isolated half-bridge BDC, it remains unclear which device family (SiC MOSFET vs. Si IGBT) becomes the thermal bottleneck under realistic cooling paths, and how much additional loss can be tolerated before junction limits are reached.

This approach is thermal-first. To compare a commercial SiC MOSFET (SCT50N120) with a commercial Si IGBT (Infineon IKY150N65EH7) at 25°. Total loss is taken strictly from port powers (avoiding double-counting). Then, measuring heatsink inflow to obtain the sink-share β (the fraction of loss that actually loads the sink). With measured sink and hot-junction temperatures, the physical sink-to-ambient resistance $R_{\theta\mathrm{sa}}^{\mathrm{phys}}$was inferred for each rig and the hot-junction loss share α, which captures where the limiting heat is generated and how it couples through$(R_{\theta\mathrm{jc}} + R_{\theta\mathrm{cs}})$. A report of steady-state temperatures is presented, a normalized figure of merit (junction rise per kilowatt, $\Delta.T_{\mathrm{j}}/\mathrm{kW}$), extra-loss headroom to a target junction limit, and junction-temperature transients.

One family-level $R_{\theta\mathrm{sa}}^{\mathrm{phys}}$ explains both buck and boost on each platform (IGBT $\approx 0.43K/W$, MOSFET $\approx 0.63K/W$) withhold-out errors on the order of a degree. Normalized results are clear: reverse power flow with the MOSFET is the harshest thermally (largest $\Delta.T_{\mathrm{j}}/\mathrm{kW}$); forward flow with the IGBT is the most benign, and in the IGBT boost, the antiparallel-diode path limits performance (the hot junction nearly tracks the sink). These translate directly into guidance: improve. $R_{\theta\mathrm{cs}}$ and $R_{\theta\mathrm{sa}}$ where they matter most, and use control levers (dead-time tuning, synchronous freewheeling) to gain headroom.

1.2. Contributions and Novelty

Compared with prior studies that mainly focus on efficiency or device-level loss breakdown [1–5,7–12], the main novelties of this work are:

- Thermal-first, loss-clean workflow. We adopt a port-power-based definition of total converter loss and measure the heatsink inflow with a dedicated sensor, which allows us to separate where heat is generated (junctions, magnetics, wiring) from how it is removed via the measured sink-share. This avoids double-counting and yields a thermally consistent picture of the converter.
- Operating-point-agnostic thermal metrics. We introduce normalized, family-level metrics—junction rise per kilowatt ($\Delta.T_{\mathrm{j}}/\mathrm{kW}$), temperature sensitivity to loss, and extra-loss headroom to a target junction limit—that enable fair comparison between SiC and IGBT legs even when their bus voltages, switching frequencies, and absolute power levels differ.
- Family-level cooling parameter with validation. We show that a single physical sink-to-ambient resistance per hardware family accurately predicts both buck and boost modes, with hold-out errors on the order of one degree. This level of agreement is obtained without case-by-case tuning of thermal parameters, which is not reported in typical converter comparison studies.
- Identification of the dominant thermal bottleneck and practical fixes. Our analysis reveals that MOSFET

reverse power flow is the dominant thermal limiter, whereas the IGBT leg operates with much lower normalized junction rise. We quantify how improvements in and, together with control levers such as dead-time tuning and synchronous freewheeling, can translate into additional thermal headroom.

Section 2 outlines the converter and thermal framework (port-power loss, β, $R_{\theta sa}^{phys}$, α). Section 3 details the models, operating points, and calibration/validation. Section 4 presents steady-state and transient results, normalized comparisons, and headroom/sensitivity. Section 5 concludes with design guidance.

2. Converter and Thermal-Analysis Methodology

2.1. Topology and Signals

This study is about a non-isolated half-bridge bidirectional buck–boost converter, as shown in (Fig. 1). The leg uses two actively gated devices (T_1, T_2) with antiparallel diodes (D_1, D_2), a series inductor on the energy-transfer path, and split DC-link capacitors. A shared ground simplifies gate driving and measurements, and short dead time prevents shoot-through.

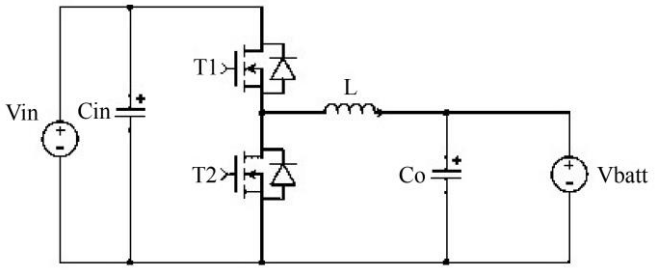

Fig. 1 Non-isolated half-bridge bidirectional DC–DC converter topology

The same hardware supports both directions of power flow. The choice of which Device is pulse-width modulated selects the operating mode; the complementary Device's body/antiparallel diode provides the freewheeling path.

In Buck (forward power flow), Power moves from the high-voltage port to the low-voltage port (Fig. 2). Device. T_1 is the actively switched leg while T_2 remains off. During the time of T_1, the inductor current rises; when T_1 turns off, the inductor releases its energy to the low-voltage bus through D_2.

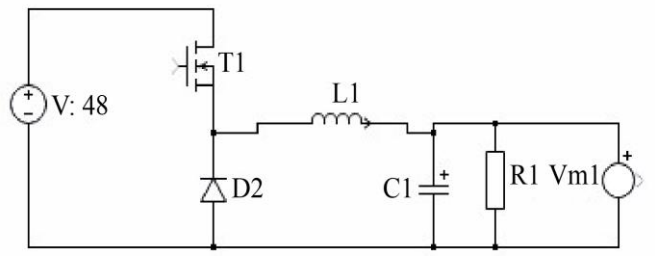

Fig. 2 Buck (forward) operation: T_1 is PWM-controlled, and freewheeling occurs via D_2.

In Boost (reverse power flow), energy flows from the low-voltage side up to the high-voltage side (Fig. 3). Device. T_2 is pulse-width modulated and T_1 is kept off. While T_2 is on, the inductor stores energy from the low-voltage source; when T_2 turns off, that energy is delivered to the high-voltage bus through D_1.

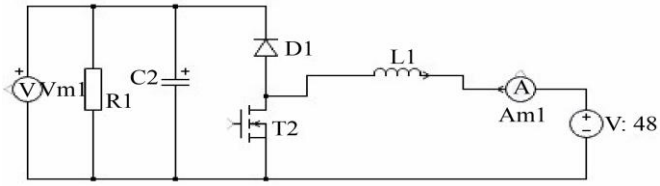

Fig. 3 Boost (reverse) operation: T_2 is PWM-controlled, and freewheeling occurs via D_1

Unless stated otherwise, the conditions in Table 1 were used (see Section 3). The SiC MOSFET leg operates at 48V and 25kHz; the IGBT leg at 400V and 20kHz; both with duty $D = 0.5$, identical passives, and direction-specific loads. Voltages and currents are sampled at the DC-side capacitors on each port. Buck mode take P_{in} from the high side and P_{out} from the low side; in Boost, the roles are swapped. Scalar quantities (power, efficiency, temperature) are averaged over the last 200ms after transients have settled.

2.2. Loss and Thermal Model

Total converter loss defined purely from port powers,

$$P_{\text{loss,tot}} \triangleq P_{\text{in}} - P_{\text{out}} = (V_{\text{in}} I_{\text{in}}) - (V_{\text{out}} I_{\text{out}}), \qquad (1)$$

And use this as the single source of truth. Device-level probes (switch/diode) are then used only to explain where losses occur (conduction, switching, reverse recovery). Probe losses do not add to heatsink inflow, which prevents double-counting; the heat-flow sensor on the sink serves as a thermal cross-check.

Because some loss is dissipated outside the leg (e.g., in magnetics, copper, wiring, and control), the measured heatsink inflow defines the sink-share

$$P_{\text{sink}} = \beta\, P_{\text{loss,tot}}, \qquad 0 \le \beta \le 1. \qquad (2)$$

With the sink temperature T_s and ambient T_{amb}, the physical sink-to-ambient resistance is

$$R_{\theta sa}^{\text{phys}} = \frac{T_s - T_{\text{amb}}}{\beta\, P_{\text{loss,tot}}}. \qquad (3)$$

This separates the cooling hardware performance ($R_{\theta sa}^{\text{phys}}$) from the portion of loss that actually heats the sink (β).

Let $R_{\theta jc}$ be the junction-to-case resistance of the limiting device path (MOSFET switch; IGBT switch in buck; IGBT diode in Boost), and $R_{\theta cs}$ the case-to-sink resistance. The hotter junction is modeled as

$$T_j^* = T_{\text{amb}} + \alpha\, P_{\text{loss,tot}} \left(R_{\theta\text{jc}} + R_{\theta\text{cs}}\right) + \beta\, P_{\text{loss,tot}}\, R_{\theta\text{sa}}^{\text{phys}} \quad (4)$$

Where $\alpha \in [0,1]$ is the inferred share of total loss that raises the hottest die, coupled through $(R_{\theta\text{jc}} + R_{\theta\text{cs}})$. Given (T_j^*, T_s) and known $(R_{\theta\text{jc}}, R_{\theta\text{cs}})$, it solved for α per operating case.

The steady-state relations in (3)–(4) are paired with compact RC ladders derived from vendor transient thermal impedance $Z_\theta(t)$ to capture dynamics. With step inputs $P_{\text{dev,hot}} = \alpha P_{\text{loss,tot}}$ and $P_{\text{sink}} = \beta P_{\text{loss,tot}}$, the transient junction temperature is

$$T_j^*(t) = T_{\text{amb}} + \left(Z_{\theta,\text{j}\to\text{c}} * P_{\text{dev,hot}}\right)(t) + \left(Z_{\theta,\text{s}\to\text{a}} * P_{\text{sink}}\right)(t), \quad (5)$$

Where $*$ denotes convolution and $Z_{\theta,\text{s}\to\text{a}}$ represents the sink-to-ambient path through $R_{\theta\text{sa}}^{\text{phys}}$ and the sink's heat capacity. The time-to-limit t_{lim} It is the first time. $T_j^*(t)$ reaches the specified $T_{j,\text{max}}$.

2.3. Metrics, Checks, and Assumptions

Because processed power differs across technologies and operating points, the report presents operating-point-agnostic metrics:

$$\Delta T_j/\text{kW} = \frac{T_j^* - T_{\text{amb}}}{P_{\text{proc}/1}}, \quad (6)$$

$$\frac{\text{d}T_j}{\text{d}P} = \alpha\,(R_{\theta\text{jc}} + R_{\theta\text{cs}}) + \beta\, R_{\theta\text{sa}}^{\text{phys}}, \quad (7)$$

with $P_{\text{proc}} = \min(P_{\text{in}}, P_{\text{out}})$ at steady state. Extra-loss headroom to a design limit $T_{j,\text{target}}$ is

$$\Delta P_{\text{max}} = \frac{T_{j,\text{target}} - T_j^*}{\text{d}T_j/\text{d}P}. \quad (8)$$

The verification is (i) power balance. $P_{\text{in}} - P_{\text{out}}$ against the sum of device/passive probes within $\pm 5\%$, and (ii) thermal consistency by confirming $P_{\text{sink}} \approx \beta P_{\text{loss,tot}}$ and the ordering $T_j^* > T_s > T_{\text{amb}}$ (within sensor resolution). Because the MOSFET and IGBT legs are exercised at different buses and switching frequencies, by emphasizing normalized metrics ($\Delta T_j/\text{kW}$, $\text{d}T_j/\text{d}P$) to enable fair comparison independent of absolute processed power.

3. Simulation Setup, Data, and Calibrated Thermal Parameters

3.1. Environment and Tool Flow

All studies were run in PLECS at $T_{\text{amb}} = 25$ using temperature-aware loss models for the semiconductors. Port powers measured at the DC capacitors are used as the single source of truth for total loss. $P_{\text{loss,tot}} = P_{\text{in}} - P_{\text{out}}$. A heat–flow probe on the leg heatsink reports the fraction of converter loss that actually enters the sink. Post-processing in MATLAB reconciles electrical loss with the measured temperatures and extracts the physical thermal parameters (Section 3.5).

3.2. Devices Under Test (DUTs)

The same half-bridge power stage is populated with:

- SiC MOSFET: Rohm SCT50N120 (1200 V class, body diode).
- Si IGBT: Infineon IKY150N65EH7 (650 V class, antiparallel diode).

Datasheet $E_{\text{on/off}}(V, I, T)$ tables parameterize switching energy; vendor transient thermal impedance $Z_\theta(t)$ is mapped to compact RC ladders for junction–case and sink dynamics. Gate levels, gate resistances, and dead time follow vendor guidance and are held constant within each device family.

3.3. Electrical Operating Points and Signals

To remain faithful to the recorded data, the original operating points reused the measurement locations. Voltages and currents are sensed at each DC port; scalar values (powers, efficiencies, temperatures) are averaged over the last 200ms after electrical and thermal transients settle.

Table 1. Electrical parameters used in all test cases.

Parameter	Setting
High-side bus (MOSFET / IGBT)	48V / 400V
Battery side (MOSFET / IGBT)	48V / 400V
Inductor L_1	1.2mH
DC-link capacitors C_1, C_2	33.83 µF, 8.33 µF
Load R (forward / reverse)	1Ω / 5Ω
Switching frequency (MOSFET / IGBT)	25kHz / 20kHz
Duty cycle D	0.5
Ambient temperature T_{amb}	25° C

3.4. Thermal Boundary Conditions

By using compact thermal paths with datasheet junction–case resistances and a common interface resistance:

$$R_{\theta\text{jc}}^{\text{MOSFET}} = 0.55K/W,$$
$$R_{\theta\text{jc}}^{\text{IGBT(switch)}} = 0.19K/W,$$
$$R_{\theta\text{jc}}^{\text{IGBT(diode)}} = 0.26K/W,$$
$$R_{\theta\text{cs}} = 0.20K/W.$$

Device limits for time-to-limit checks are $T_{j,\text{max}} = 200$ (SiC) and 175 (Si IGBT).

3.5. Calibrating the Cooling Path and Hot-Junction Share

Because not all converter loss heats the sink (magnetics, copper, wiring, control), a per-case sink share is defined:

$$P_{\text{sink}} = \beta\, P_{\text{loss,tot}}, \qquad \beta \in [0,1],$$

measured by the heat–flow probe. With sink temperature T_s and ambient T_{amb}, the physical sink–ambient resistance is

$$R_{\theta\mathrm{sa}}^{\mathrm{phys}} = \frac{T_s - T_{\mathrm{amb}}}{\beta\, P_{\mathrm{loss,tot}}}. \tag{9}$$

The limiting junction temperature is modelled as

$$T_j^* = T_{\mathrm{amb}} + \alpha\, P_{\mathrm{loss,tot}}\left(R_{\theta\mathrm{jc}} + R_{\theta\mathrm{cs}}\right) + \beta\, P_{\mathrm{loss,tot}}\, R_{\theta\mathrm{sa}}^{\mathrm{phys}} \tag{10}$$

Where $\alpha \in [0,1]$ is the inferred hot-junction loss share (switch for MOSFET; switch in IGBT buck; diode in IGBT boost). Solving (9)–(10) with measured $(P_{\mathrm{loss,tot}}, T_s, T_j^*)$ yields β, $R_{\theta\mathrm{sa}}^{\mathrm{phys}}$, and α.Fitted values from the recorded runs.

Table 2. Per-case calibration (sink share β, physical $R_{\theta\mathrm{sa}}$, and hot-junction share α).

Case	β	$R_{\theta\mathrm{sa}}^{\mathrm{phys}}$ [K/W]	α
MOSFET buck	0.615	0.641	0.294
MOSFET boost	0.999	0.626	0.545
IGBT buck	0.076	0.427	0.039
IGBT boost	0.427	0.430	0.000

A single value per family fits all runs with near-zero error, indicating consistent cooling hardware per rig:

$$R_{\theta\mathrm{sa}}^{\mathrm{phys}} \approx \begin{cases} 0.63K/W & (\mathrm{MOSFETrig}), \\ 0.43K/W & (\mathrm{IGBTrig}). \end{cases}$$

3.6. Transient Modelling and Reporting

A dynamic model with vendor-derived RC ladders for the junction–case path and a lumped heatsink capacity. The limiting junction trajectory $T_j^*(t)$ It is reported that over 600, and t_{lim} is defined as the first time $T_j^*(t)$ reaches $T_{j,\max}$. Under the tested conditions, none of the four cases hit the device limit within 600s.

3.7. Normalized Metrics and Headroom

To compare devices that process different power levels, based on operating-point-agnostic metrics:

$$\Delta T_j/\mathrm{kW} = \frac{T_j^* - T_{\mathrm{amb}}}{P_{\mathrm{proc}}/1kW}, \tag{11}$$

$$\frac{\mathrm{d}T_j}{\mathrm{d}P} = \alpha\left(R_{\theta\mathrm{jc}} + R_{\theta\mathrm{cs}}\right) + \beta R_{\theta\mathrm{sa}}^{\mathrm{phys}}. \tag{12}$$

with $P_{\mathrm{proc}} = \min(P_{\mathrm{in}}, P_{\mathrm{out}})$ at steady state. The extra-loss headroom to a chosen limit $T_{j,\mathrm{target}}$ is :

$$\Delta P_{\max} = \frac{T_{j,\mathrm{target}} - T_j^*}{\mathrm{d}T_j/\mathrm{d}P}.$$

These quantities let us translate temperatures into design margin directly.

3.8. Calibration Check (visual)

Fig. 4 plots T_s against $\beta\, P_{\mathrm{Loss,tot}}$ for all runs. The fitted slope equals $R_{\theta\mathrm{sa}}^{\mathrm{phys}}$, confirming the expected linear relation in (9).

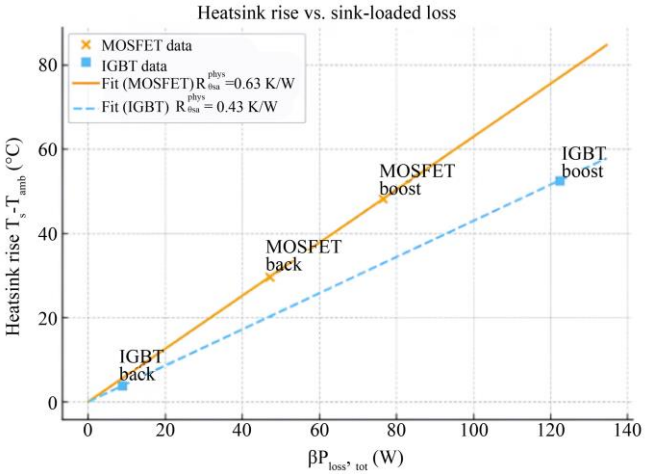

Fig. 4 Heatsink rise versus $\beta P_{\mathrm{loss,tot}}$ with fitted line; slope = $R_{\theta\mathrm{sa}}^{\mathrm{phys}}$

3.9. Model Validation and Generalization Across Modes

To check generalization, a single $R_{\theta\mathrm{sa}}^{\mathrm{phys}}$ Per family fits on one mode and predicts the other. Mean errors are small (Table 3), supporting a family-level cooling parameter.

Table 3. Hold-out validation: fit on one mode, predict the other (mean error over held-out case).

Family	Fit on	$R_{\theta\mathrm{sa}}$ (K/W)	Mean error (°C)
IGBT	boost → buck	0.427	T_s: -0.34, T_j^*: -0.34
IGBT	boost → buck	0.430	T_s: +0.02, T_j^*: +0.00
MOSFET	buck → boost	0.641	T_s: +1.16, T_j^*: +1.17
MOSFET	boost → buck	0.626	T_s: -0.71, T_j^*: -0.72

The IGBT rig shows sub-degree agreement ($|\mathrm{meanerror}| \leq 0.34$). The MOSFET rig also transfers well, with a small, repeatable offset ($\approx \pm 1$). Therefore, quote family-level values with conservative uncertainty bands from the hold-out residuals:

$$\mathrm{R}_{\theta\mathrm{sa}}^{\mathrm{phys}} \approx \begin{cases} [\mathrm{l}]0.63\mathrm{K/W}(\pm 0.02\mathrm{K/W}, \pm 1.2), \mathrm{fortheMOSFETrig} \\ [\mathrm{l}]0.43\mathrm{K/W}(\pm 0.01\mathrm{K/W}, \pm 0.35), \mathrm{fortheIGBTrig} \end{cases}$$

4. Results and Discussion

This is a presented steady-state and transient thermal behavior for both legs (SiC MOSFET and Si IGBT) in buck and boost at $T_{\mathrm{amb}} = 25$. Unless noted, total loss uses port powers ($P_{\mathrm{loss,tot}} = P_{\mathrm{in}} - P_{\mathrm{out}}$); the heatsink share is $\beta =$

$P_{\text{sink}}/P_{\text{loss,tot}}$, and T_j^* follows (10) with calibrated $(R_{\theta\text{sa}}^{\text{phys}}, \alpha)$ from Table 2.

4.1. Electrical Summary (Context)

Table 4 lists the measured port powers. Because the IGBT cases process substantially more absolute power, relying on normalized thermal metrics for fair cross-family comparisons.

Table 4. Electrical summary (port powers).

Case	P_{in}(W)	P_{out}(W)	η (%)	P_{loss}(W)
MOSFET buck	1108.8	1032.2	93.09	76.6
MOSFET boost	1502.4	1425.8	94.90	76.6
IGBT buck	7800.0	7683.0	98.50	117.0
IGBT boost	25120.0	24833.6	98.86	286.4

4.2. Calibrated Cooling and Hot-Junction Share

Solving (9)– (10) per case yields a physical sink–ambient resistance and a hot-junction share that are consistent across modes for each family (Table 2). Two takeaways:

- Family-consistent cooling. One value of $R_{\theta\text{sa}}^{\text{phys}}$ describes each rig: about 0.63K/W for the MOSFET setup and 0.43K/W for the IGBT setup. The difference reflects the mechanical sink/airflow, not the semiconductors.
- Who runs hottest (and why). In MOSFET–Boost, $\alpha \approx 0.545$ with $\beta \approx 1$ indicates substantial switch/diode-related heating (switching energy plus body-diode conduction during dead time). In IGBT–Boost, $\alpha \approx 0$ and $T_j^* \approx T_s$ Point to a sink-dominated rise where the antiparallel diode is the main heater and the junction sits close to the sink.

4.3. Normalized Junction Rise per Kilowatt

It is a comparison of thermal severity using the normalized rise $\Delta.T_j/\text{kW} = (T_j^* - T_{\text{amb}})/(P_{\text{proc}}/1kW)$. MOSFET boost is highest at 55.6°C/kW, followed by MOSFET buck at 45.6°C/kW, while IGBT boost and buck are far lower at 2.12°C/kW and 0.73°C/kW, respectively.

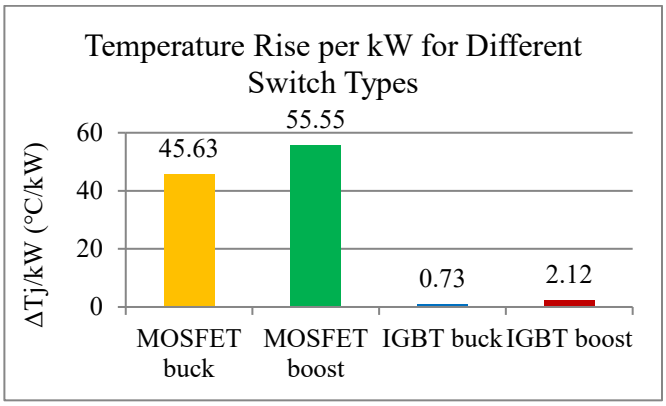

Fig. 5 Normalized junction rise per kilowatt, ΔT_j/kW

4.4. Headroom to a Target Junction Limit

The temperature sensitivity to loss is $\mathrm{d}T_j/\mathrm{d}P = \alpha\,(R_{\theta\text{jc}} + R_{\theta\text{cs}}) + \beta\, R_{\theta\text{sa}}^{\text{phys}}$.Using $T_{j,\text{target}} = 110$, the extra-loss headroom is $\Delta P_{\max} = (T_{j,\text{target}} - T_j^*)/(\mathrm{d}T_j/\mathrm{d}P)$. MOSFET–boost is the limiting case (about 5.6W headroom); IGBT–buck has the largest margin (about 1.66kW).

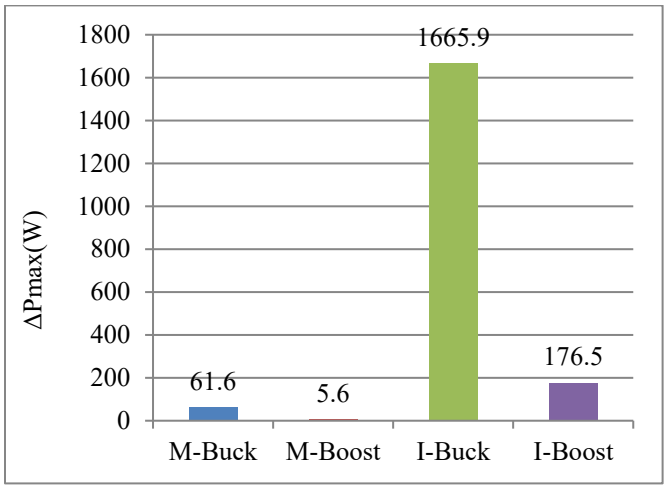

Fig. 6 Extra-loss headroom to $T_{j,\text{target}} = 110$.

4.5. Junction-Temperature Transients

Transient behavior is computed with vendor-derived RC ladders (junction–case) and a lumped sink capacity. Over a 600s window, none of the four cases reach the device limit (all. $t_{\text{lim}} = \infty$ under the tested conditions), which aligns with the steady-state headroom.

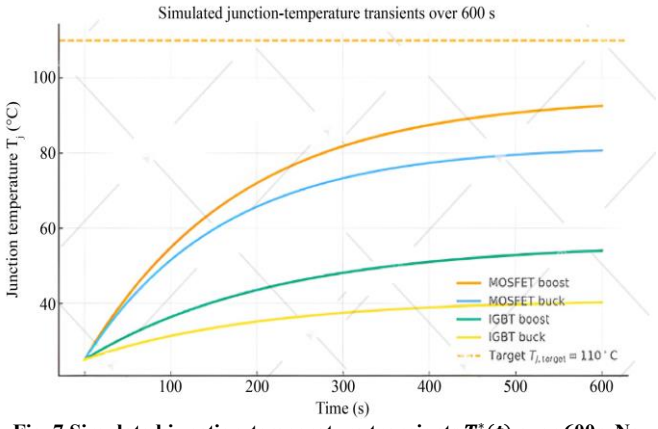

Fig. 7 Simulated junction-temperature transients $T_j^*(t)$ over 600s. No case hits $T_{j,\max}$ in this window

4.6. Cooling Trade-Off Analysis

Fig. 8 shows how improvements in $R_{\theta\text{cs}}$ and $R_{\theta\text{sa}}^{\text{phys}}$ affect junction temperature for the limiting case (MOSFET boost). Reducing interface resistance provides diminishing returns, while sink improvements offer linear benefits across the range.

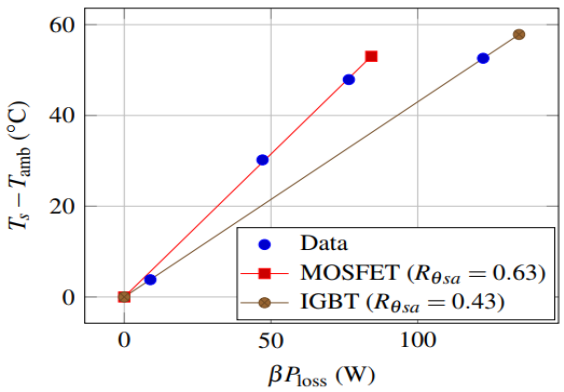

Fig. 8 Cooling trade-off sweep: sensitivity of T_j to improvements in $R_{\theta cs}$ and $R_{\theta sa}^{phys}$.

4.7. Design Implications

Three practical takeaways:

- Reverse flow is the MOSFET bottleneck. The combination of switching energy and body-diode intervals in Boost drives the worst $\Delta T_j/\mathrm{kW}$ and the smallest margin. The most effective levers are dead-time tuning, lower. $R_{\theta cs}$ (TIM quality and mounting pressure), and reduced$R_{\theta sa}$ (bigger sink/airflow). Synchronous freewheeling can further cut diode heating.
- The IGBT rig benefits from a cooler path. With $R_{\theta sa}^{phys} \approx 0.43 K/W$ and modest α, both IGBT modes show very low normalized rise. In Boost, the antiparallel diode dominates sink heating ($\alpha \approx 0$, $T_j^* \approx T_s$), suggesting a lower-Q_{rr} A diode or synchronous conduction would yield the largest thermal dividend.
- Normalize before you compare. Because families ran on different buses and switching frequencies, raw temperatures are not directly comparable. The normalized metrics ($\Delta T_j/\mathrm{kW}$, $\mathrm{d}T_j/\mathrm{dP}$) detach device behaviour from absolute power and make heatsink/airflow sizing and control trade-offs transparent.

4.8. Comparison with Existing Work and Discussion of Improvements

The results above can be interpreted in the context of existing bidirectional converter studies and thermal management techniques. Prior comparisons of SiC and Si devices in BDCs and EV chargers [4,11] primarily report efficiency improvements, switching-energy reductions, or case-temperature trends under selected operating points. These works provide valuable insight into the device-level trade-offs but generally treat thermal behavior as a secondary outcome of electrical design. In contrast, the present study is thermal-first: all conclusions are drawn from port-power loss, measured heatsink inflow, and inferred junction temperatures.

This measurement-based workflow explains why we can fit a single physical sink-to-ambient resistance per hardware family with sub-degree error across both buck and boost modes (Table 2 and Table 3). By explicitly measuring the sink-share and inferring the hot-junction loss share, we avoid the need to assume that all converter loss flows into the heatsink, which is a common simplification in earlier lumped-parameter approaches [7,12]. As a result, the normalized junction rise per kilowatt and the loss-to-temperature sensitivity reported here are tightly linked to the actual thermal path of the hardware, rather than to idealized datasheet values.

The "better" performance of the proposed approach relative to the state of the art lies therefore in the quality and usefulness of the thermal information, not only in absolute temperatures. For example, identifying MOSFET boost as the worst case with the smallest extra-loss headroom (Fig. 6) immediately indicates that reverse power flow in the SiC leg should drive heatsink sizing and control optimization. At the same time, the very low normalized values observed for the IGBT leg show that, for the chosen hardware, the IGBT path operates with a generous thermal margin. Such Device- and mode-aware insight is difficult to obtain from efficiency-only comparisons or from analyses that do not separate.

Finally, the proposed normalized metrics make it easier to map our findings onto other published operating points. Even though the bus voltages and switching frequencies in [1–5,8–12] differ from those considered here, designers can use our values to estimate junction-temperature rise and headroom for their own processed power levels, provided that the cooling path is comparable. In this sense, the present work complements existing efficiency-driven studies by offering a practical, measurement-grounded thermal lens for comparing SiC and Si technologies in bidirectional DC–DC converters.

5. Conclusion

This paper shifts the comparison between SiC MOSFETs and Si IGBTs from an efficiency-only view to a thermal perspective. Instead of summing device probe losses, total loss is computed from the difference between input and output power, and measuring how much of that heat actually loads the heatsink (the sink share, β). Using the measured sink and junction temperatures, estimated the physical sink-to-ambient resistance for each setup and the share of loss produced in the hottest device path (α). A single thermal parameter per hardware family explains both buck and boost cases with very small errors, which enables fair comparisons using normalized metrics such as junction rise per kilowatt.

The main result is clear: MOSFET boost is the limiting case. It shows the largest normalized temperature rise and the smallest thermal headroom. The IGBT cases run noticeably cooler on a per-kilowatt basis. In practice, the best levers are to tune dead time, use synchronous freewheeling where appropriate, and improve the thermal path by lowering interface and sink resistances. Cooling should be sized based on the tightest headroom case, not on efficiency alone.

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