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Original Article

Thermographic Analysis for Failure Time Estimation of PV-qZMLI

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Abstract *- A very commendable progress has been observed in the grid-connected photovoltaic quasi-Z-Source multilevel inverters (PV-qZMLI) in recent years. The advantages offered by the topology and the ever-increasing importance of its implementation in PV applications, electric vehicles, automobiles, spacecrafts, military, and other critical applications have led to testing the veracity of its lifetime and reliable operation. To assess the reliability, estimation of failure rates is of paramount importance. The temperature factor is essential to estimate the failure rate of the component. Since 53% of total failures in the inverters are reported to occur due to overheating, thermal management is pivotal. Therefore, this chapter contributes to the thermographic analysis of PV-qZMLI. The data is collected by introducing variations in input voltage, operating time, and operating states to track the thermal profile of each component in the proposed topology. The thermographs taken using a FLIR thermal imaging camera are presented, and the case studies are discussed for each operating condition. Also, the failure rates are calculated for varying operating conditions, and the results are elucidated.*

Keywords *- Failure rate, Impedance Network, Quasi Z-Source Inverter, Reliability, Shoot-through, Temperature, Thermograph.*

1. Introduction

In recent decades, there has been a rapid increase in global energy demand due to the fast depletion of nonrenewable fossil fuels and their increased cost. As solar energy is globally available, it can be used to meet the ever-increasing energy requirements. “Efficient use of available solar energy is closely linked to the chosen converter topology. Grid-connected multilevel Photovoltaic (PV) inverter systems are widely utilized in large-scale renewable energy applications, as they offer features such as enhanced efficiency, minimized distortion in input current, and the elimination of the step-up transformer. In addition, independent voltage control and individual maximum power point tracking are possible as the cascaded multilevel inverters need separate DC sources that can be obtained from a PV string [1, 2].

The qZMLI has always been a vital constituent of the failures in a PV-based power generation system, and it is mainly due to the failure of switching devices, Impedance network elements, and dc-link capacitors. The reliable operation of the PV inverters is very important as the characteristics, such as efficiency, modularity, and reliability, cannot be compromised from the industry point of view [3, 4]. The modification in the structure of the topology and applied modulation techniques can lead to improvement in efficiency and modularity. However, the reliability is given a higher emphasis in critical applications since the proposed PV-qZMLI has impedance network elements and additional shoot-through operating states. The voltage stress across the switches and other operating components is obvious in PV-qZMLI. Thermal stress, Mechanical, and electrical stresses are the primary factors contributing to the failure of these devices [5, 6]. Among these factors, thermal stress emerges as the most common cause of failure. As the inverters used in the PV applications are mainly H-Bridge type, the switching devices like IGBTs or MOSFETs are involved in hard switching during the power conversion process. In the case of hard switching, the voltage and current transitions occur in the switching devices. During the turn-on condition, the current starts to rise and reaches a steady state, and vice versa happens during the turn-off condition. Therefore, switching loss is obvious, which, in conjunction with electromagnetic interference, increases the temperature of the switching devices. Hence, it is necessary to mitigate the switching losses to improve the efficiency. The choice of material, the modulation strategy, and the operating frequency have their shadow reflected on the losses of the switching devices [7, 8].

To assess reliability, thermal analysis can be employed to identify the thermal performance of power switching devices and impedance network elements. Infrared Thermography is a method used to identify the presence of thermal aberrations

and monitor the thermal distribution in power electronic components. In this technique, contactless thermal measurements are taken to identify the thermal behaviour of the proposed inverter under various operating conditions.

This paper is elucidated into the following sections. Section 1 provides a sufficient introduction to why thermal analysis is important. Section 2 deals with how the reliability of the proposed system is affected due to thermal stress. Section 3 discusses various case studies under varying operating conditions, and Section 4 provides the numerical results of temperature factor estimation and the impact on MTTF. The final Section concludes the remarks of the thermographic analysis of the proposed inverter.

2. Temperature as a Reliability Affecting Parameter

2.1. Reliability Definition

Reliability can be understood as the probability that an item operates correctly, without failure, for a defined period and under specified conditions [9, 10]. Alternatively, it is often quantified by the number of failures occurring within a given timeframe and mathematically expressed as

$$R(t) = (T > t),\ t \geq 0 \qquad (1)$$

2.2. Reliability Objectives

1. Prevention and reduction of the failure occurrences.
2. Diagnosis and Alleviation of the root cause of failures.
3. Establishing methods of failure management if failure factors are not resolved.
4. Investigation and Estimation of the reliability of new topologies.

2.3. Standards of Reliability

The process of reliability prediction is based on failure rate data provided in internationally accepted military and commercial standards. As part of this process, equipment manufacturers must conduct reliability analyses using recognized standards, such as MIL-HDBK-217, Bellcore / Telcordia (SR-332), NSWC-06/LE10, China 299B, and RDF 2000.

2.4. Reliability Metrics

For a non-repairable item, reliability is nothing but the probability of the device/component over the expected lifetime, if only one failure can occur. The metrics used are failure rate / hazard rate and Mean Time to Failure (MTTF). It represents the instantaneous probability of only one failure occurring in the entire operating lifetime. The failure rate, also referred to as the hazard rate, is defined as a function of time and represented by λ, and the Mean Time to Failure (MTTF) is estimated as $1/\lambda$. For a repairable system, reliability is expressed as the probability that no failure occurs during its expected service life, even though multiple failures may be possible. The metrics used are failure rate (λ) and Mean Time Between Failures (MTBF), which is $1/\lambda$ with the assumption that the failures occur at a constant rate [11, 12].

2.5. How does the Thermal Stress Affect Reliability?

When a power electronic switching device is operated at a higher operating frequency, heat is generated. The cyclic and repeated transitions in the current values produce switching losses that dissipate as heat across the device, leading to a temperature rise of the device package. The generated heat is conducted through the device package, heat sink, solder joints, and ultimately dissipated into the Printed Circuit Board (PCB). Owing to the thermal resistance associated with the package components and the heat sink, the package will be hotter than the PCB. Since the heat flows from the heat sink to the PCB through the soldered joints, the temperature rises, but is not greater than the device package. The power cycling results in temperature differences and applies shear stresses in soldered joints.

In a greater number of operating power cycles, it will eventually lead to cracks in the solder joints and cause failure of the system. Therefore, it is very important for a power electronic system to withstand a greater number of power cycles. The thermal cycling, in combination with mechanical vibrations, may increase the failure rate. The magnitude of the applied load has a significant impact on temperature rise; therefore, the system must be operated within its rated capacity during both transient and steady-state operation. Given that the reliability of power electronic components is strongly influenced by temperature, thermal analysis plays a critical role in system design and is essential during the design phase [13]. The proposed PV-qZMLI is mainly subjected to voltage stress during shoot-through operation. The component voltage stress is reflected as a temperature rise, and the failure rate of the components will increase. Finally, the reduced lifetime of the component occurs due to an increase in the Mean Time To Failure (MTTF).

3. PV-Quasi Z-Source Multilevel Inverter

Quasi Z-source multilevel inverter is an emerging and suitable candidate for photovoltaic power generation systems since it features separate DC sources, better performance parameters, and a transformer-less structure. Multiple single-phase quasi-Z-Source Inverters (qZSI) can be connected in series to create a cascaded H-bridge quasi-Z-source Multilevel Inverter (qZMLI). For each cascaded module, the structure and the control method are similar. Higher voltage levels and improved power quality can be achieved b a series connection, and high reliability can be obtained due to its modular structure [4, 14, 15]. The qZMLI blends all the advantages of qZSI and multilevel inverter, which mainly includes single-stage power conversion and improved power quality. Figure 1 shows the five-level PV-qZMLI.Two H-bridges of qZSI are connected in series to form a five-level qZSI.

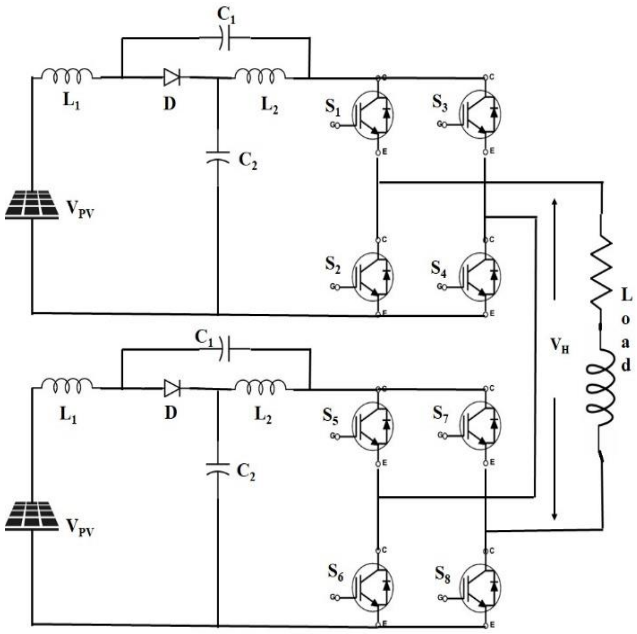


Fig. 1 Photovoltaic quasi-Z-source multilevel inverter (PV-qZMLI)

3.1. Functional Modes of QZSI

The Quasi-Z-Source Inverter (QZSI) operates in two fundamental modes: Shoot-Through (ST) and Non-Shoot-Through (NST). During the shoot-through mode, the quasi-Z-source network boosts the input voltage supplied by the Photovoltaic (PV) source, causing the inverter to function as a current source. In the non-shoot-through mode, the boosted DC voltage is converted into an AC output, and power is delivered to the load. The overall output voltage, denoted as v_H is obtained as the sum of the voltages generated by the individual H-bridge modules v_{H1} and v_{H2}.

3.1.1. Non-Shoot through Mode

As illustrated in Figure 2, the diode is short-circuited, and the gating signals applied to the switches are identical to those used in a conventional voltage-source inverter. Under this operating condition, the available DC-link voltage is supplied to the H-bridge inverter and subsequently converted into an AC output.

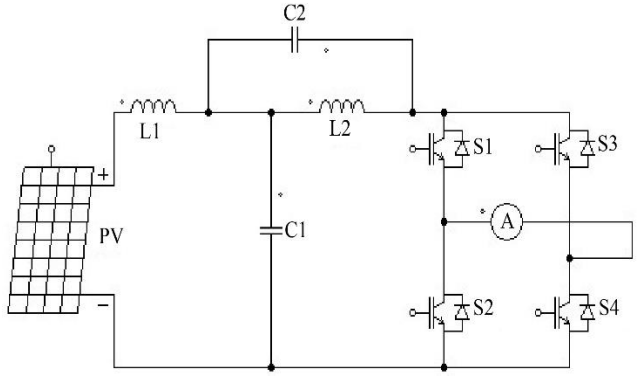


Fig. 2 NST mode of QZSI

3.1.2. Shoot through Mode

As shown in Figure 3, the switches within the same inverter leg are simultaneously turned on for a brief duration. However, the PV source is not short-circuited because of the presence of the LC network. During this stage, the applied voltage is boosted. The DC-link voltage corresponds to the boosted input voltage, with the boost factor governed by the shoot-through duty ratio.

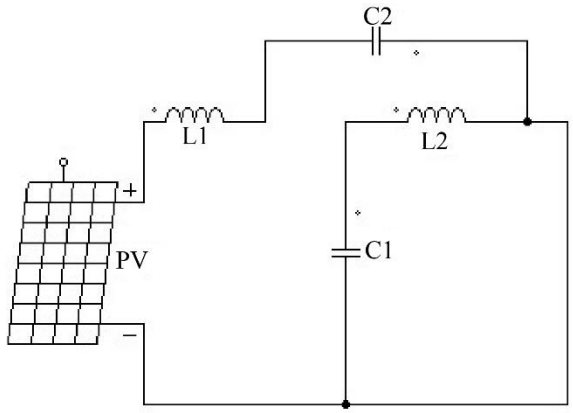


Fig. 3 ST of QZSI

Table 1. Parameters of PV-qZMLI

System Variables	Specifications
Operating frequency, fs	10 kHz
Shoot-through duty ratio, D	0.25
Source Voltage, VDC	0 - 60 V
DC link voltage, VPN	145 V
Inverter output Power, Vo Io	500VA
Modulation Index, M	0.85
Boost factor, B	1.8
Inductor, L1, L2	3mH
Capacitor, C1, C2	2.2µF

A hardware circuit of the projected qZSI is developed. The hardware circuit is shown in Figure 4, and the parameters are listed in Table 1. Two solar panels of specified rating are connected as separate inputs to each stage of the qZMLI. The quasi-impedance network connected to the PV panels, as well as the H-bridges, acts as an interface between them in each individual stage of the qZMLI. The Printed Circuit Board (PCB) is designed, and the components that belong to a quasi-impedance network, H-bridges, and driver circuit are fabricated. Phase-Shifted Pulse-Width Amplitude Modulation (PS-PWAM) signals are generated using the MATLAB / Xilinx interface.

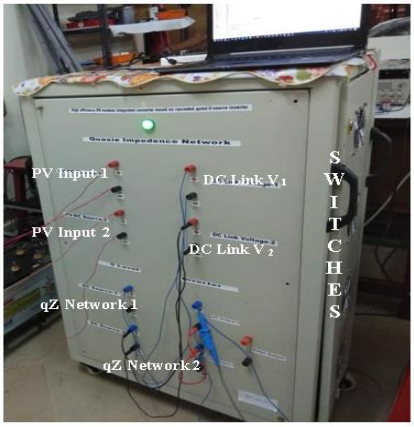
These gating signals are applied to the switching devices of the H-bridge inverters through an FPGA-based SPARTAN-3E processor. The output terminals of the individual H-bridges are connected in cascade to produce a multilevel voltage

waveform. Figure 4 illustrates the five-level output voltage obtained from the PV-fed quasi-Z-source Multilevel Inverter (PV-qZMLI). For an input voltage of 10-60 V, the output voltage is boosted to 1.8 times the applied voltage.

4. Case Study for Thermal Analysis of PV-qZMLI

The inverter components are subjected to a wide range of temperature variations during their operation. The temperature profile of the inverter components must be taken into analysis to obtain an insight into the reliability of the inverter. The thermal history of each component elucidates the inverter performance and its dependency on operating states and ambient conditions.

Since the proposed inverter operates in an additional operating state called the shoot-through state, the switching devices are subjected to high voltage stress. The temperature rises, and its changes are analysed using Infrared Thermography. An attempt has been made to collect the data for tracking the temperature profile under various operating conditions using a FLIR thermal imaging camera. Three cases, such as variation of input voltage, change in operating states, and variation in time of operation, have been accounted for in the analysis.



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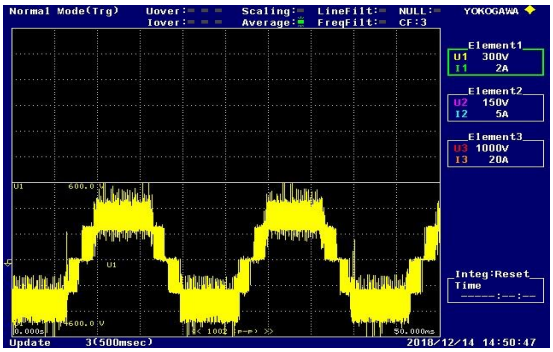
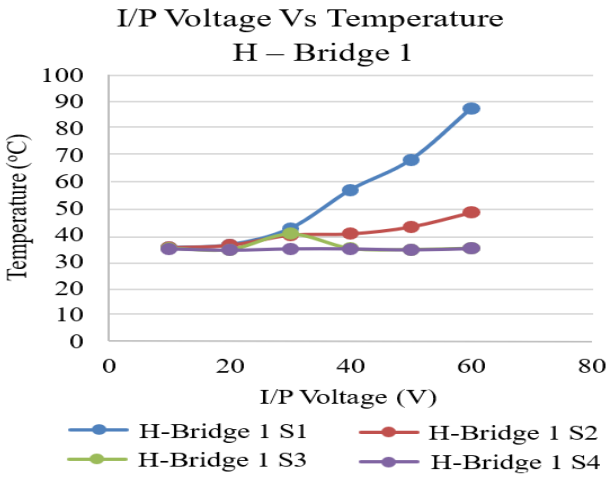


(b)

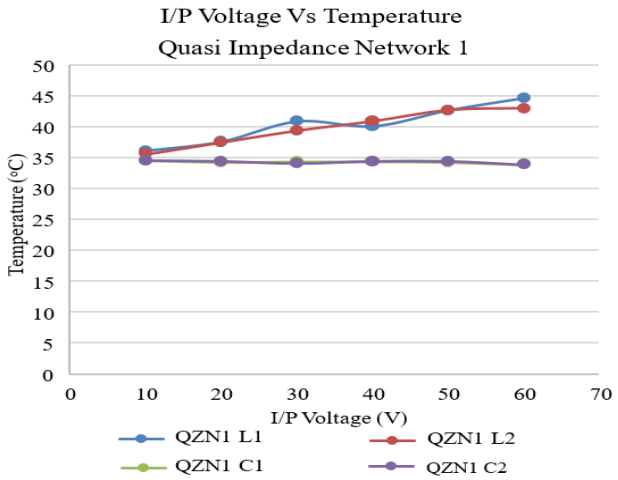
Fig. 4 Hardware implementation of PV-qZMLI; (a) Hardware setup, and (b) Output voltage.

4.1. Case I: Variation of Input Voltage

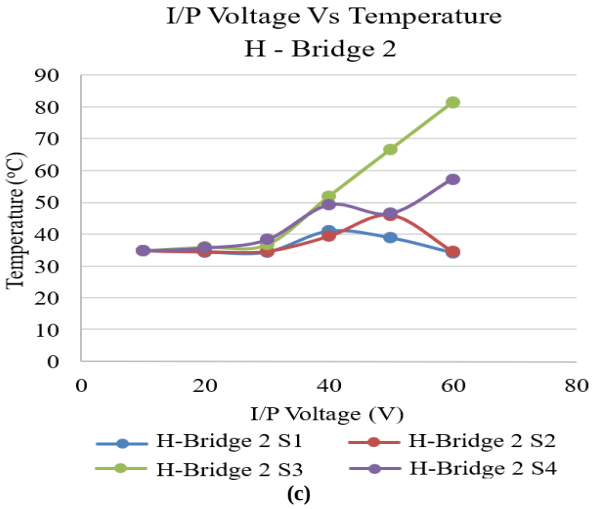
When the voltage at the source port changes from low voltage to high voltage, the temperature variation of H-Bridge 1, H-Bridge 2, components of quasi-impedance network 1, and quasi-impedance network 2 of the proposed topology are observed and recorded. The temperature profile of the switches S_1, S_2, S_3, and S_4 of H-Bridge 1 is shown in Figure 5 (a). It can be inferred from Figure 5 that the highest temperature of 87.3 ˚C is recorded by switch S_1 for an input voltage of 60V. A temperature difference of 52.3 ˚C resulted when switch S_1 operated at 10 V input. The switches S_3 and S_4 remain at the same operating temperature with a variation of ±0.5ºC when the voltage at the source port varies from 10 to 60 V. It can be inferred from Figure 5 (a) that the highest temperature of 87.3 ˚C is recorded by switch S_1 for a feeding voltage of 60V. A temperature difference of 52.3 ˚C resulted when switch S_1 operated at a 10 V source. The switches S_3 and S_4 remain at the same operating temperature with a variation of ±0.5ºC when the source terminal voltage varies from 10 to 60 V.



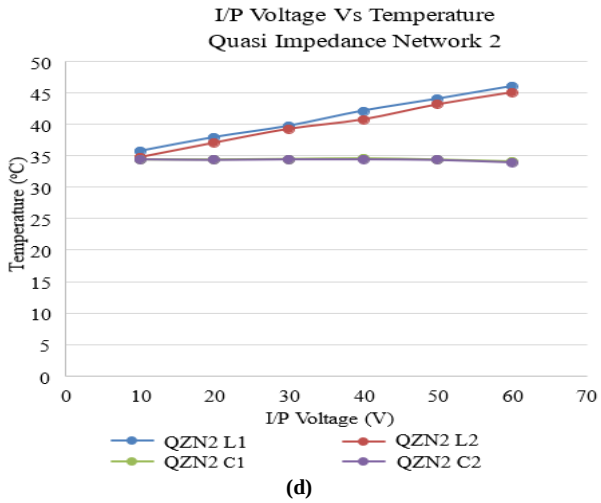
(a)



(b)



(c)



(d)

Fig. 5 Input Voltage Vs Temperature, (a) H-Bridge 1, (b) qZN1, (c) H-Bridge 2, and (d) qZN2.

The temperature variations in the first quasi-Z-source network components, such as L_1, L_2, C_1, and C_2, are shown in Figure 5 (b). The inductors L_1 and L_2 show a temperature difference of 8 °C, and the capacitors C_1 and C_2 do not reflect much temperature variation when the source port voltage changes from 10 to 60 V per bridge.

The temperature of the switches S_1, S_2, S_3, and S_4 of H-bridge 2 is shown in Figure 5 (c). It can be inferred from the Figure that the highest temperatures, 81.4 °C and 57.3 °C, are reached by S_3 and S_4 at an input voltage of 60V. A temperature difference of 46.6 °C and 22.5 °C has been observed when S_3 and S_4 operate at 10 V input. There is a slight increase in the temperature of S_1 and S_2 when the input voltage varies from 10 to 60 V.

The temperature variations observed in the components of the second quasi-Z-source network 2, such as L_1, L_2, C_1, and C_2, are depicted in Figure 5 (d). The inductors L_1 and L_2 show a temperature difference of 10 °C, and the capacitors C_1 and C_2 do not have any significant temperature variation when operated with a source voltage of 10 – 60 V per bridge.

4.2. Case II: Change in Operating States

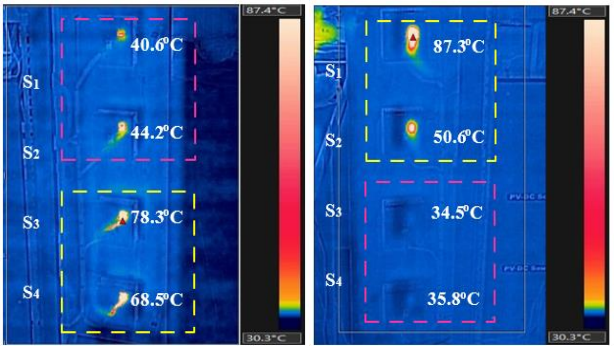
Thermal analysis is done during ST and NST operation at 60 V of the proposed topology. During the ST, switches S1 and S2 of H-bridge 1, as well as switches S3 and S4 of H-bridge 2, experience the highest electrical stress, resulting in a peak temperature of 87.3°C. The corresponding thermal images illustrating this behaviour are presented in Figure 6(a) and Figure 6 (b). In the Figures, the yellow boxes refer to the shoot-through state, and the pink boxes refer to the NST state. The observed temperature rise is attributed to the ST interval, during which the upper and lower switches within the same inverter leg conduct simultaneously in order to boost the input voltage. As the inverter behaves like a current source, the first leg of the H-Bridge 1 and the second leg of the H-Bridge 2 result in increased stress across the switches, leading to the temperature rise.

4.3. Case III: Change in Operating Time

In this case, the temperature variations are recorded for two sets of terminal voltages, 10 V and 60 V per bridge, after 10 minutes of operation. Figure 7 (a) and (b) show the thermographs of the H-bridges 1 and 2, respectively, after 10 minutes of operation with an input terminal voltage of 10 V per bridge. It can be observed that the switches S_1 and S_2 of H-bridge 1 show an increased temperature during 10 V input applied for 10 minutes.

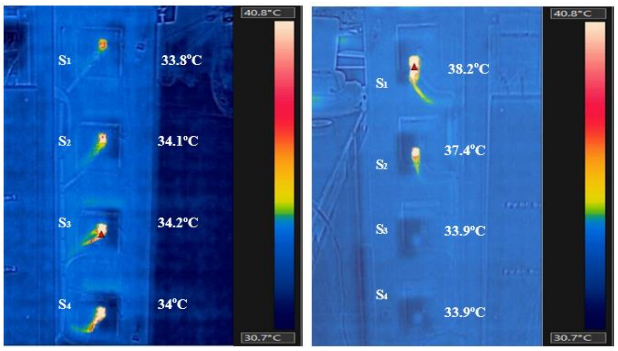
Since these two switches are often involved in the ST operation and connected in series with the source inductor, this temperature variation is significant. The switches S_3 and S_4 of the H-bridge 2 do not show much variation in temperature. This behaviour can be attributed to the relatively low applied input voltage and the correspondingly small source current, which together result in reduced electrical stress on the power devices. For both bridges, the temperature increment is about 5 °C. Figure 8 (a) and (b) show the thermographs of the qZN_1 and qZN_2, respectively, after 10 minutes of operation with an input voltage of 10V per bridge.

For 10V operation, the inductors are subjected to a temperature variation of around 5 °C. Various temperature readings of L_1 and L_2 are marked on the thermographs. Since the inductors are involved in boost operation during shoot-through, they suffer high current stress. So, the internal resistance of the inductor causes more voltage drop, increased power loss, and thus leads to increased temperature of the semiconductor devices. Figures 8 (c) and (d) show the thermal images of qZN1 – C1 and qZN1 – C2 for a 10 V input after 10 minutes of operation. Figure 9 (a) and (b) show the thermal images of qZN2 – C1 and qZN2 – C2 for a 10 V input after 10 minutes of operation.



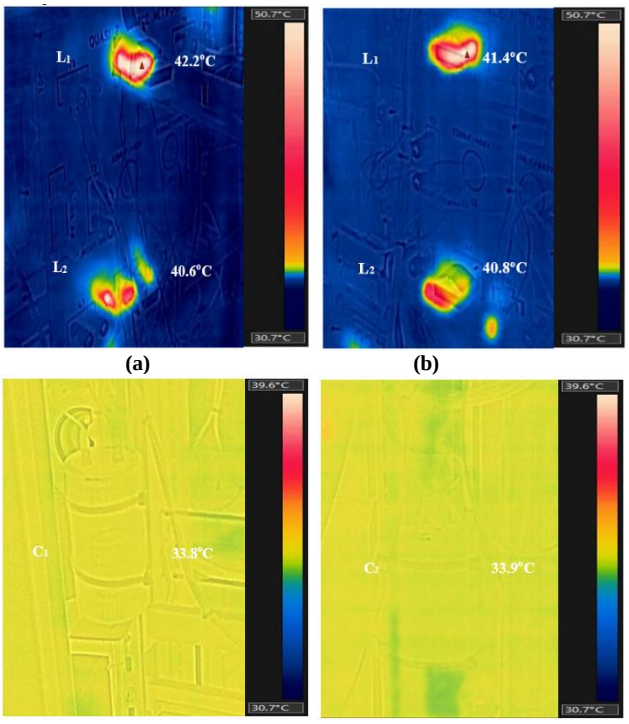
(a) (b)

Fig. 6 Thermographs: (a) H-Bridge 1, and (b) H-Bridge 2.



(a) (b)

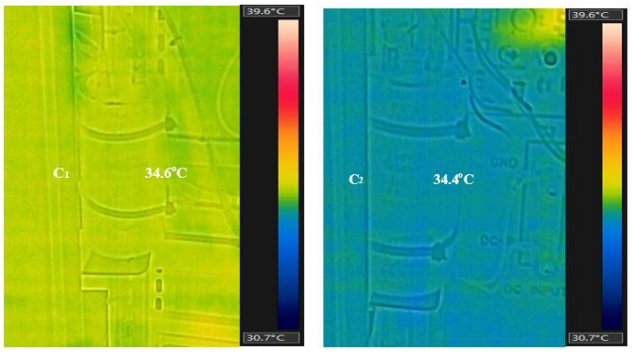
Fig. 7 For 10 V input after 10 minutes of operation: (a) H-Bridge 1, and (b) H-Bridge 2.



(a) (b)

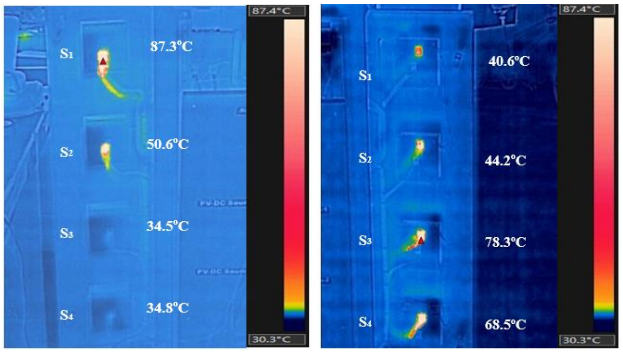
(c) (d)

Fig. 8 For 10 V input after 10 minutes of operation, L_1 and L_2: (a) qZN_1, (b) qZN_2, (c) $qZN_1 – C_1$, and (d) $qZN_1 – C_2$.



(a) (b)

Fig. 9 For 10 V input after 10 minutes of operation



(c) (d)

Fig. 10 For 60 V input after 10 minutes of operation: (a) H-Bridge 1, and (b) H-Bridge 2.

From the observations, all the capacitors show temperature readings of 34 °C, which was the room temperature while observing the thermographs. Since these elements are not involved in the shoot-through and boosting operation, they remain at the same temperature throughout the entire operation of the circuit. Figures 10 (a) and (b) show the thermographs of the H-bridge 1 and 2, respectively, after 10 minutes of operation with an input voltage of 60 V per bridge. It can be observed that the switches S1, S2 of H-bridge 1 and switches S3, S4 of H-bridge 2 are showing increased temperature of 87.3ºC, 50.6ºC, 78.3ºC and 68.5ºC respectively during 60 V input applied for 10 minutes.

Since these switches are involved in the shoot-through operation and also connected to the load terminals to deliver the load current, this temperature variation is observed. For both bridges, the temperature increment ranges from 16 ˚C to 46 ˚C, which results in the cooling of the switches to avoid thermal stress. Figures 11(a) and (b) show the thermographs of the quasi-impedance networks 1 and 2, respectively, after 10 minutes of operation with an input voltage of 60 V per bridge. The same network under the operation of 60 V input faces a temperature rise of 15 ˚C. Figures 11 (c) and (d) show the thermal images of qZN1 – C1 and qZN1 – C2 for 60 V input after 10 minutes of operation. Figures 12 (a) and (b) show the thermal images of qZN2 – C1 and qZN2 – C2 for 60 V input after 10 minutes of operation.

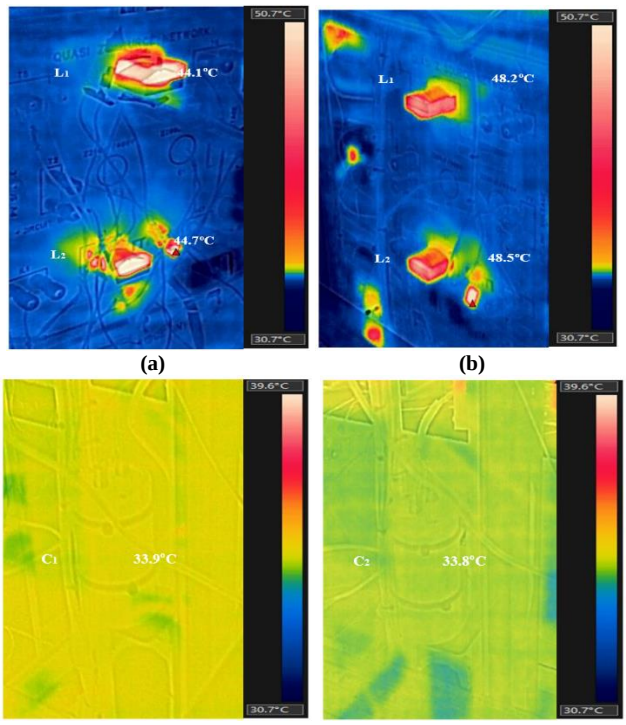
From the observation, all the capacitors show an average temperature of 34.5 °C, which is just above the room temperature, while taking the thermographs with 60 V input. Since these elements are not involved in the shoot-through and boosting operation, they remain at the same temperature throughout the operation and are not affected much.

5. Failure Rate Estimation of PV-Qzmli based on Thermography

For the proposed PV-fed quasi-Z-source multilevel inverter (PV-qZMLI), the failure rates of the switches, capacitors, diodes, and inductors are estimated using the reliability database specified in MIL-HDBK-217. The failure rate calculation for each component incorporates several contributing factors, including environmental factor (πE), temperature factor (πT), quality factor (πT), application factor (πA), contact construction factor (πC), electrical stress factor (πS), capacitance variation factor (πCV), and base failure rate (λb) [16]. The overall system failure rate is given by 31.0672 failures/million hours. The MTTF is calculated as 469704 hours for the proposed PV-qZMLI. It can be observed that the capacitor is the component where the failure rate estimation is not based on the temperature factor. The thermography images reveal the same in all three test cases/operating conditions. When the failure rates are estimated for the highest temperature achieved by switch S1 (87.3°C from 52.3 °C), S3 (81.4 °C from 57.3 °C), and a temperature deviation of 10 °C in the inductors of the impedance network, the temperature factor π_T changes for the temperature variation, and the same is updated from the MIL-HBK 217 database. Therefore, the failure rates are estimated as follows for the varied temperature factors. The failure rate of the inductor and the capacitor remains the same as per the previous case, as the temperature difference is not accounted for variation up to 10 °C. Therefore, the overall system failure rate and MTTF for the proposed PV-QZMLI are given in Table 2.

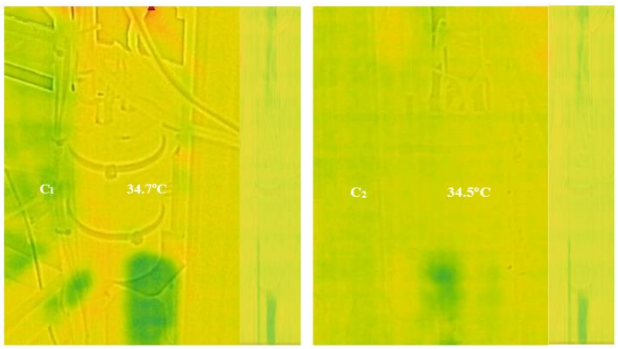
Table 2. Failure rate and MTTF computation

Component / System / Parameter	Empirical Formula for Failure Rate (Failures / 106 hours)	Failure Rate (Failures / million hours)	
		Initial Temperature	Highest Temperature
Switch	$\lambda_S = \lambda_b\pi_T\pi_A\pi_E\pi_Q$	1.2512	2.4576
Diode	$\lambda_D = \lambda_b\pi_T\pi_S\pi_C\pi_Q\pi_E$	0.1449	0.23184
Capacitor	$\lambda_C = \lambda_b\pi_{CV}\pi_E\pi_Q$	0.000875	0.000875
Inductor	$\lambda_L = \lambda_b\pi_C\pi_Q\pi_E$	3.3×10^{-5}	3.3×10^{-5}
System	$2\lambda_{PV} + 8\lambda_S + 2\lambda_D + 4\lambda_C + 4\lambda_L$	21.293	31.0672
Mean Time to Failure (Hours)	$1/\lambda$	469704	321882



(a) (b) (c) (d)

Fig. 11 For 60 V input after 10 minutes of operation, L_1 and L_2 (a) qZN_1, (b) qZN_2, (c) $qZN_1 - C_1$, and (d) $qZN_1 - C_2$.



(a) (b)

Fig. 12 For 60 V input after 10 minutes of operation, qZN_2, (a) C_1, and (b) C_2.

Table 3. Failure rate and MTTF results

Operating Condition	Temperature Factor (πT)	Failure Rate (Failures / Million Hours)	Mean Time to Failure (Hours)
Initial Temperature (Room Temperature)	1.62	21.293	469704
Highest Temperature (87.3 °C)	3.2	31.0672	321882

From Table 3, it can be observed that the temperature factor increases by 3.2 for switches. Since large temperature variations are observed in the switches, more emphasis is given to their impact on device lifetime. Also, it is evident that the increase in temperature has increased the failure rate of the entire system by a factor of 1.45, and hence the mean time to failure reduces, which in turn implies the reduced lifetime of the proposed system.

6. Conclusion

For the thermal analysis of the proposed inverter, a FLIR thermal imaging camera was used to capture the temperature of various components during operation. Three test cases, such as an increase in input voltage, an increase in time of operation, and shoot-through operation of the switching devices, were considered for thermal study. The results show that during all three cases, the inductors of both the impedance networks, switches S_1 and S_2 of H-bridge 1, and switches S_3 and S_4 of H-bridge 2, showed increased thermal stress at high operating voltages and longer operating time periods. The capacitors do not show significant temperature changes. The failure rate estimated for the normal operating condition is 21.29 failures/million hours, and with the highest temperature achieved, it is 31.0672 failures/million hours. It can be concluded that the failure rate increases and the mean time to failure decreases from the thermography of the PV-qZMLI. Thus, a prediction is made for the possible failure time of the proposed system.

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References

[1] Dongsen Sun et al., "A New Grid-Connected PV System based on Cascaded H-Bridge Quasi-Z Source Inverter," *2012 IEEE International Symposium on Industrial Electronics*, Hangzhou, China, pp. 951-956, 2012. [CrossRef] [Google Scholar] [Publisher Link]

[2] Baoming Ge et al., "Minimized Quasi-Z Source Network for Single-Phase Inverter," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, USA, pp. 806-811, 2015. [CrossRef] [Google Scholar] [Publisher Link]

[3] Dongsen Sun et al., "Analysis and Control of Quasi-Z Source Inverter with Battery for Grid-Connected PV System," *International Journal of Electrical Power and Energy Systems*, vol. 46, pp. 234-240, 2013. [CrossRef] [Google Scholar] [Publisher Link]

[4] Anh-Vu Ho, and Tae-Won Chun, "Single-Phase Modified Quasi-Z-Source Cascaded Hybrid Five-Level Inverter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 5125-5134, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[5] N. Robert Sorensen et al., "Thermal Study of Inverter Components," *IEEE Journal of Photovoltaics*, vol. 3, no. 2, pp. 807-813, 2013. [CrossRef] [Google Scholar] [Publisher Link]

[6] Anna V. Andonova, and Nikolay L. Hinov, "Thermographic Analysis of a Bridge Power Converter," *Journal of Electrical Engineering*, vol. 65, no. 6, pp. 371-375, 2014. [CrossRef] [Google Scholar] [Publisher Link]

[7] Anup Anurag, Yongheng Yang, and Frede Blaabjerg, "Thermal Performance and Reliability Analysis of Single-Phase PV Inverters with Reactive Power Injection Outside Feed-In Operating Hours," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 870-880, 2015. [CrossRef] [Google Scholar] [Publisher Link]

[8] Michael T. Zhang, Milan M. Jovanovic, and Fred C. Lee, "Design and Analysis of Thermal Management for High-Power-Density Converters in Sealed Enclosures," *Proceedings of APEC 97 - Applied Power Electronics Conference*, Atlanta, GA, USA, pp. 405-412, 1997. [CrossRef] [Google Scholar] [Publisher Link]

[9] Saiful Islam et al., "Investigating Performance, Reliability and Safety Parameters of Photovoltaic Module Inverter: Test Results and Compliances with the Standards," *Renewable Energy*, vol. 31, no. 8, pp. 1157-1181, 2006. [CrossRef] [Google Scholar] [Publisher Link]

[10] Giovanni Petrone et al., "Reliability Issues in Photovoltaic Power Processing Systems," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7 pp. 2569-2580, 2008. [CrossRef] [Google Scholar] [Publisher Link]

[11] Alan Ristow et al., "Development of a Methodology for Improving Photovoltaic Inverter Reliability," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2581-2592, 2008. [CrossRef] [Google Scholar] [Publisher Link]

[12] Sairaj V. Dhople et al., "Integrating Photovoltaic Inverter Reliability into Energy Yield Estimation with Markov Models," *2010 IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Boulder, CO, USA, pp. 1-5, 2010. [CrossRef] [Google Scholar] [Publisher Link]

[13] Yanfeng Shen et al., "Wear-Out Failure Analysis of an Impedance-Source PV Microinverter based on System-Level Electrothermal Modeling," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3914-3927, 2019. [CrossRef] [Google Scholar] [Publisher Link]

[14] Joel Anderson, and Fang Z. Peng, "A Class of Quasi-Z-Source Inverters," *2008 IEEE Industry Applications Society Annual Meeting*, Edmonton, AB, Canada, pp. 1-7, 2008. [CrossRef] [Google Scholar] [Publisher Link]

[15] Ayman Ayad, and Ralph Kennel, "A Comparison of Quasi-Z-Source Inverters and Conventional Two-Stage Inverters for PV Applications," *EPE Journal*, vol. 27, no. 2, pp. 43-59, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[16] *Military Handbook, Reliability Prediction of Electronic Equipment*, USA Department of Defense, MILHDBK-217F, vol. 2, no. 10.1, 1990. [Google Scholar]