

Original Article

Analysis of Fifteen and Thirteen-Level Novel Cascaded Inverter Design

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Abstract - Purpose: This study aims to develop enhanced Cascaded Multilevel Inverter (CMLI) topologies for 15- and thirteen-level operation with a reduced number of switches, while maintaining low Total Harmonic Distortion (THD) and high efficiency for applications that include energy from renewable sources and Electric Vehicle (EV) drives. **Design/methodology/approach:** The proposed inverters employ asymmetric DC sources and a reduced switch architecture combined with novel Level-Shifted Pulse-Width Modulation (LSPWM). The system was modelled and validated using MATLAB/Simulink simulations to examine the output voltage quality, efficiency, harmonic performance, and switching loss. **Findings:** The simulation results confirm that the 13-level and 15-level inverter designs achieve efficiencies above 94% with significantly lower switch counts compared to those of conventional cascaded H-bridge inverters. The proposed topologies yielded THD values of 8.08% and 7.39% for 13- and 15-level inverters, respectively. The switching losses and voltage stress are condensed through the reduced-switch approach, resulting in a compact and cost-effective system. **Originality/value:** Unlike typical CHB inverters, which need a significant number of switches and independent sources, the proposed architectures provide high-quality output with fewer components. A comparative analysis demonstrated that reduced-switch LSPWM-based designs improve the harmonic performance, efficiency, and cost-effectiveness. Therefore, they are appropriate for EV motor drives and Photovoltaic (PV) applications.

Keywords - Cascaded Multilevel Inverter (CMLI), Level-Shifted Pulse Width Modulation (LSPWM), Total Harmonic Distortion (THD), Efficiency, Electric Vehicle (EV) drives, Photovoltaic (PV).

1. Introduction

Multi-Level Inverters (MLIs), which provide less Total Harmonic Distortion (THD), reduced voltage stress, and increased efficiency, are important for medium-to high-power conversion. They can be applied to industrial motor control, Electric Vehicle (EV) drives, and renewable energy systems. Multilevel Inverters (MLIs) are essential for medium- and high-power energy conversion because they can create stepped output waveforms with lower dv/dt stress, less harmonic distortion, and higher efficiency.

Traditional MLI designs include clamped diode structures, flying capacitors, and Cascaded H-Bridge (CHB) structures, which rely on numerous semiconductor switches, resulting in increased complexity, cost, and switching losses. Minimizing the switch count while maintaining performance metrics, such as low THD, high efficiency, and robust voltage handling, is crucial for practical and compact power converter designs. One promising way to achieve this balance is to use asymmetric DC sources combined with an enhanced pulse-width modulation strategy. This study proposes novel fifteen- and thirteen-level cascaded Multi-Level Inverter (CMLI)

topologies that address the above challenges. Compared with conventional CHB structures, the proposed designs require significantly fewer active switches and gate drivers. The proposed system employs a Novel Level-Shifted Pulse-Width Modulation (NLSPWM), supported by mathematical analysis and implemented digitally to optimize the switching performance. The simulation and experimental validation of the system demonstrated the effectiveness of this reduced-switch configuration in achieving an acceptable THD, high output quality, and overall cost efficiency. In a conventional H-bridge inverter, the output waveform is a square wave oscillating between +V_{dc} and -V_{dc}. Harmonic analysis showed a high total harmonic distortion (THD) of 48.34%, indicating the substantial presence of unwanted harmonics in the output. Large output filters are typically required to mitigate such harmonics. The primary issue of the MLI two-level H-bridge can be resolved in two ways. One such method (Thiyagarajan, 2019; Devi & Srivani, 2015). This approach reduces the voltage fluctuations typical of conventional two-level inverters by generating switching pulses using an appropriate PWM technique for controlling the inverter switches. A PWM inverter uses comparison logic to



repeatedly turn switches on and off within a single output voltage cycle. The switching occurred at a comparatively high frequency. The switching losses rise in parallel with the switching frequency. Consequently, even at lower harmonics, switching losses increased. Applications requiring medium-to-high power can take advantage of pulse-width modulated inverters. However, high voltage ratings and switching losses restrict the capacity of switching devices to function at extremely high frequencies in Applications with high power and high voltage ratings. (Babaei et al., 2014). Multi-level inverters provide a different alternative.

Multi-level inverters and industrial applications with medium and high power are needed. (Kumar et al. (2022)). The frequency and amplitude of the staircase output can be changed with appropriate control and connectivity. The output voltage is produced in steps or levels when the sources and loads are correctly connected. The systems are connected using semiconductor switches. The number of levels represents the number of steps from a negative peak to a positive peak, which can be produced at the output. Converter phases must produce at least three distinct voltage levels to be classified as multilevel inverters. The output began to resemble a sine wave as the number of levels was increased. Consequently, a multilayer inverter with multiple levels will have a very low output-voltage THD [2].

As a result, it might be possible to do away with the requirement for large filters at their output or perhaps the filter itself. (Devi and Srivani, 2015). There are several advantages of comparing multilayer inverters with conventional H-bridge inverters. One, ten, and 13, respectively. Some examples include reduced output voltage distortion, minor or non-existent filters, enhanced power quality, greater control flexibility, greater efficiency, and switches with lower voltage ratings. However, they have a number of disadvantages, such as the requirement for additional switches for multilevel inverters and distinct driver circuits for each switch.

The three most widely used topologies are the innovative cascaded, clamped diodes, and flying capacitors (Devi and Srivani, 2015). Capacitor disruption occurs in the neutral position of clamping inverters with multiple levels when the load current draws power from the neutral point, which causes unequal voltage distribution across the capacitors that are joined in series. Consequently, the switching devices experience uneven voltage stress. To solve this issue, it is necessary to use specialized voltage-balancing techniques or feed each series-connected capacitor into an independent power supply. More switches are required in a cascaded topology.

The flying capacitor topology produces varying output voltage levels through the addition or subtraction of the capacitor voltages. However, unbalanced capacitors can cause such issues. To resolve the issue, more control measures must

be established. Numerous strategies are being proposed for overcoming those constraints. In papers [3, 6, 8], in order to recommend a reduced-switch architecture with a resistive load. It consists of several switches to adjust the level and an H-bridge to select polarity. Each step of the output voltage was produced using a separate DC source. The lower voltage rating requirement for the level-selection switches is an advantage of this architecture. This architecture connects a source in series with a semiconductor switch for each level generation in parallel to another switch.

A source that is connected in series with a switch will short-circuit that specific source because the parallel switch will be forward-biased. This is the main drawback of this topology. In [4], a different reduced-switch MLI topology was proposed (Azib et al., 2023).

Level and polarity selection switches constitute this topology. This study used unequal pulse-width modulation, which is a relatively simple switching logic. Using this switching logic, the inverter output voltage may be made almost sinusoidal by adjusting the ON timings of the relevant switches to calculate the amplitude for every level. Multilevel inverters have been the subject of extensive research over the past two decades, with numerous topologies developed to improve waveform quality, reduce component count, and enhance system reliability.

Among the first multilayer designs were diode-clamped and flying capacitor inverters, but these were constrained by large switch counts and capacitor balance problems. To address these limitations, Cascaded H-Bridge (CHB) topologies have gained popularity owing to their modular structure and scalability. However, in order to reach high voltage levels, typical CHBs need several independent DC sources and power switches. To decrease the number of switches, many modifications were suggested.

A hybrid CHB construction that reduces THD but still needs 22 switches for a 13-level output has been proposed by Siddique et al. (2019). In Babaei (2008), A. García-Reyes (2022), a symmetric MLI using dual carriers, demonstrated low harmonic content but involved complex voltage-balancing circuits. Similarly, Azib et al. (2023) and H. Mansourizadeh et al (2025) present a 13-level inverter suitable for EV traction applications with moderate THD but higher implementation cost. Despite these innovations, many topologies either maintain high switch counts or compromise waveform quality. Moreover, a standard limitation across many designs is the lack of comprehensive performance evaluation, particularly in terms of voltage stress, switching loss, and cost-benefit analysis. This creates a research gap that is addressed by proposing reduced-switch MLI architectures with a holistic analysis covering THD, efficiency, switching behavior, voltage sharing, and practical cost estimates.

2. Methodology

2.1 Existing System

2.1.1. 7 Level Multilevel Inverter 7-Level, 9 Switches

Three direct current sources and a new H-bridge with five more switches in addition to four working switches are integrated in the system depicted in Figure 1 to offer seven

levels of steps for half cycles that are both positive and negative. (Liu et al. (2020)).

Decreased overall harmonic distortion, improved waveform of the output voltage, and increased efficiency. The benefits offered by a seven-level cascaded multilevel inverter encompass enhanced usage of the DC supply.

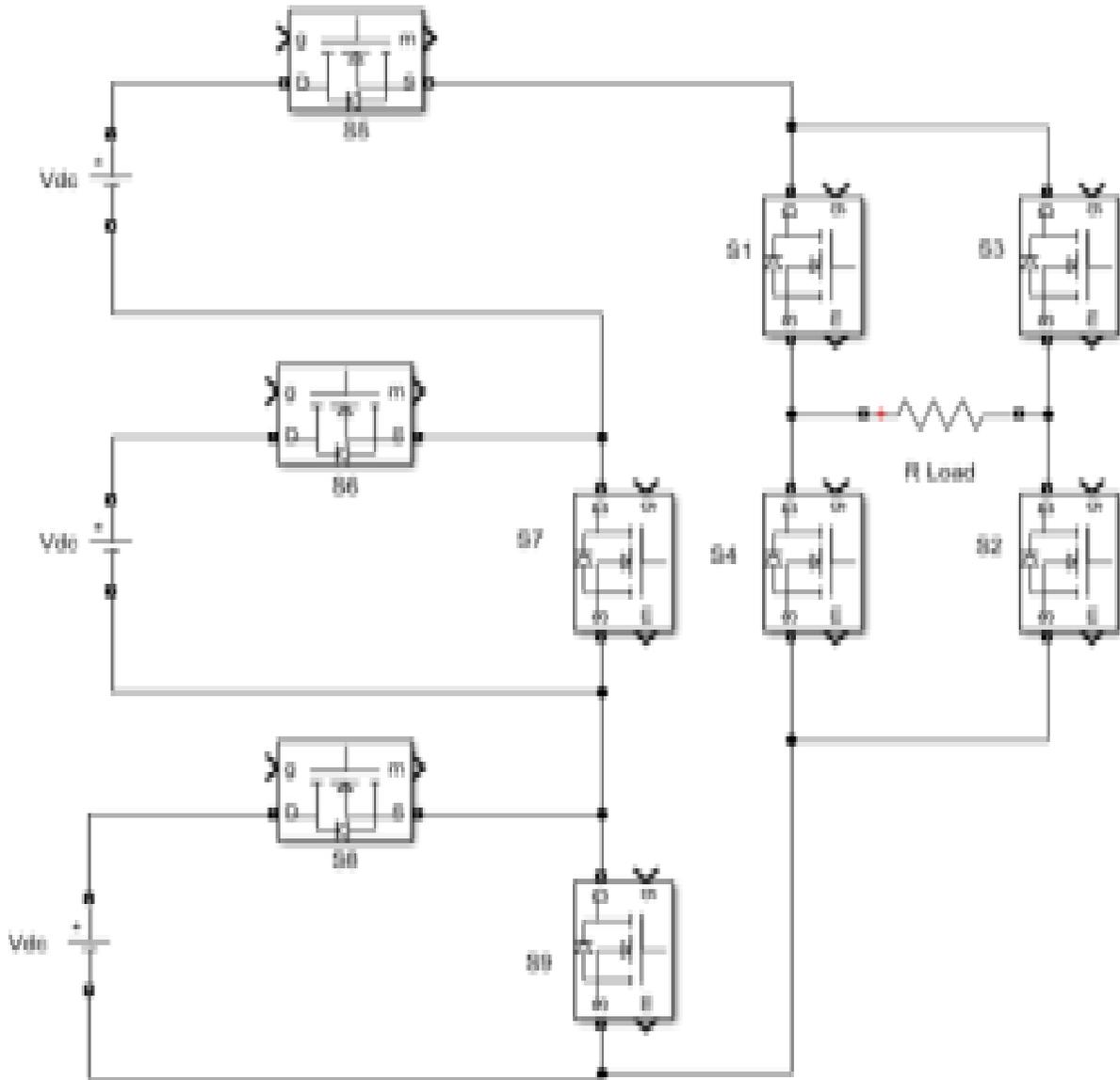


Fig. 1 9-Switch 7-level topology

Multilevel Inverter with 9 Levels

This type of inverter consists of four separate DC voltage sources (DC voltage1, DC voltage2, DC voltage3, and DC voltage4), each connected to individual switches and semiconductor devices, along with an H-bridge and multi-conversion cell. Each voltage source included one switch and one diode, connected in a cascaded manner through a circuit. These components generate only positive polarity multilevel output voltages. To produce both positive and negative

polarities, a multi-conversion cell is integrated with a single H-bridge. Figure 2 shows a multilayer inverter with nine levels. The load activates switches S1 and S2 before turning off switches S3 and S4. A first-level output voltage of +1 Vdc is produced. The load eventually has a second-level output voltage of +2Vdc after all the switches are activated. To activate the switches and reach a voltage level of +3Vdc, the process is repeated (turning off S4) to activate the switches to attain a +4Vdc voltage level.

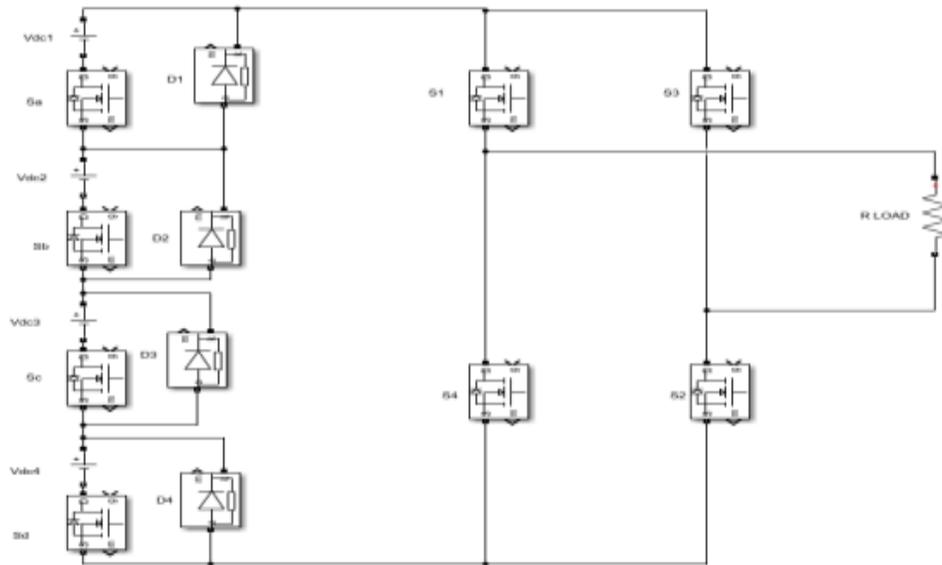


Fig. 2 Cascaded multilevel inverter with nine levels

11 Level Multilevel Inverter

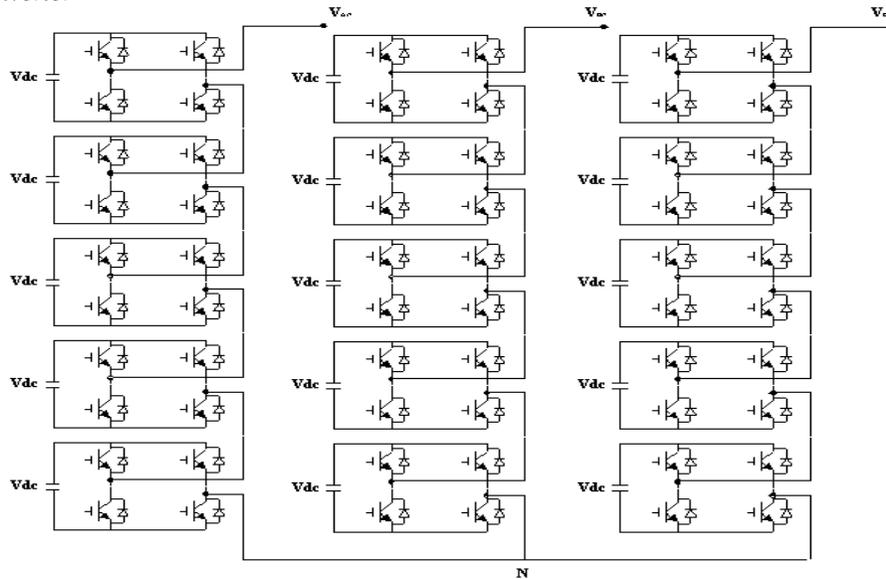


Fig. 3 Cascaded multilevel inverter with eleven levels

To achieve higher output levels, the circuit design becomes more complex, requiring the cascading of five H-bridges to produce an eleven-level output voltage. This three-phase, eleven-level inverter is optimized with fewer gate-driver circuits owing to the use of smaller power components. Figure 3 illustrates the eleven-level multilevel inverter design. The Conventional Cascaded H-Bridge Multilevel Inverter (CHB-MLI) is frequently used because of its superior output and modular design. However, it relies on multiple identical H-bridge cells, each powered by an isolated DC source, which results in a large number of switches. For an n-level output, the traditional CHB design requires power switches two (n-1). For instance, a 13-level inverter requires 24 switches, and a 15-level design requires 28 switches. This leads to high

switching losses, bulky hardware, complex controls, and increased costs. Moreover, conventional designs generally use sinusoidal PWM or space-vector modulation without significant optimization for switch reduction. These systems also suffer from voltage-stress concentration and poor cost efficiency.

2.2 Proposed System

Figure 4 illustrates that the advanced multi-level inverter has ten MOSFET power switches, six powered diodes, and three uneven sources. To create a multiple-level output in a special manner, the voltages from the three DC voltage sources were summed simultaneously. Separate switches were used to select combinations. The modified reduction switch

has a conventional H-bridge for polarity selection and many switches for level selection. By using fewer switches and Level-Shifted Pulse Width Modulation (LSPWM), as illustrated by Figure 5, the suggested approach also reduces switching losses. The harmonics diminished as the number of levels increased. A switch attached in parallel to the source performs the same function as a switch linked in series. The DC voltage sources were connected via level selection switches, producing a multistep output. Three levels of operation are possible for the H Bridge: $0 + V_{dc}$, and $-V_{dc}$.

Auxiliary switches create additional levels. Electric vehicle (EV) motor drives use a cascaded MLI. The three advantages of the novel cascaded H-bridge inverter are as follows:-

- (1) They only require fundamental frequency switching to generate voltages that are almost sinusoidal.
- (2) They rarely experience Electromagnetic Interference (EMI) or common-mode voltage.
- (3) MLI makes EVs safer and more accessible.

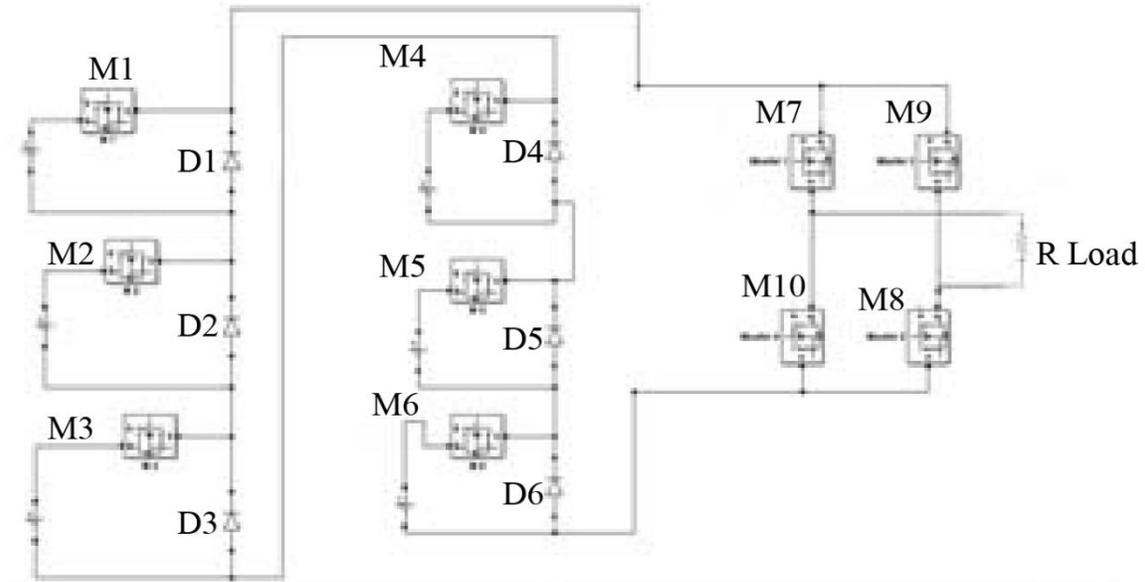


Fig. 4 13-Level cascaded multilevel inverter

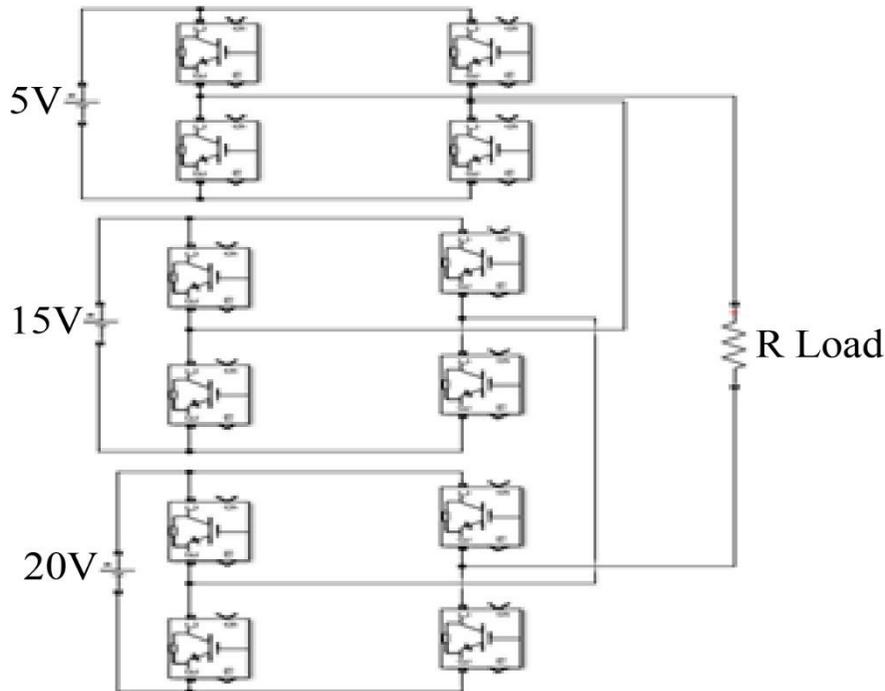


Fig. 5 15-Level cascaded multilevel inverter

The suggested system uses asymmetric DC voltage sources and fewer power switches to implement an optimised design. Instead of duplicating full H-bridge cells, a minimal combination of unipolar switches is used in conjunction with an H-bridge polarity inverter to generate the required voltage levels. For a 13-level inverter, only 10 switches are used, as shown in Figure 4, and for the 15-level configuration, only 12 switches are required, as shown in Figure 5. The switching scheme uses Level-Shifted Pulse-Width Modulation (LSPWM), which enables more efficient level generation with a better harmonic distribution. The proposed topology reduces the component count, simplifies control, minimizes switching loss, and offers a cost-effective solution without significantly sacrificing harmonic performance. The results were validated by MATLAB simulations. The proposed inverter configurations are based on a Cascaded Multilevel Inverter (CMLI) structure with an optimized switch reduction strategy. The core design consists of two primary functional blocks: (1) a level-generation module composed of reduced switches connected to the asymmetric DC voltage sources, and (2) a cascaded circuit for polarity inversion. Voltage levels in the output were determined by the quantity and intensity of the DC sources, and the switching logic was implemented. For the thirteen-level and fifteen-level designs, different combinations of source values were employed to generate discrete stepped voltages that approximated sinusoidal waveforms.

The reduced-switch topology ensures that fewer switches are activated at any given time, thus minimizing the conduction and switching losses. Novel level-shifted pulse-width modulation was executed to control the inverter operation. This technique uses multiple carrier waveforms shifted in the vertical axis and a reference sine wave to determine gate signals. The system compares the reference waveform.

$V_{ref}(t) = M_a * V_m \sin(\omega t)$ with each triangular carrier signal $V_{cr_i}(t)$, producing pulse-width-modulated outputs for the switches.

Mathematical formulation:

$$G_i(t) = 1 \text{ if } V_{ref}(t) > V_{cr_i}(t); \text{ else } 0$$

3. Simulation Results and Analysis

A thirteen-level NCHBMLI containing ten switching patterns is shown in the simulation schematic in Figure 6. Figure 7 displays the voltage waveform output of the 13-level innovative cascaded multilevel inverter. The simulation model of an innovative fifteen-level cascaded multilevel inverter having 12 switches is illustrated in Figure 8. Figure 9 depicts a 15-level innovative cascaded multilevel inverter output voltage waveform. A comparison of the FFT analysis at different levels is presented in Table 1. Comparison With Existing Reduced-Switch MLIs is displayed in Table 2.

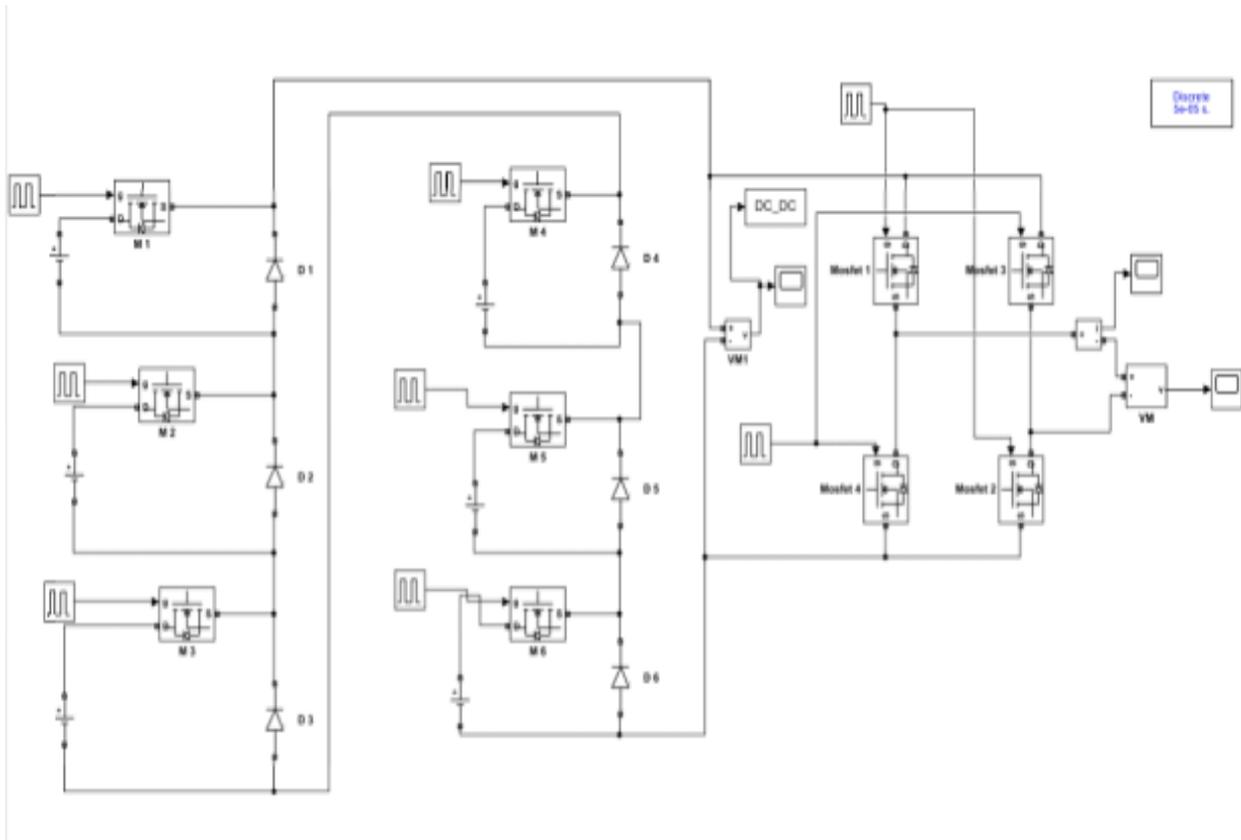


Fig. 6 Proposed 13-level novel cascaded topology's simulation diagram

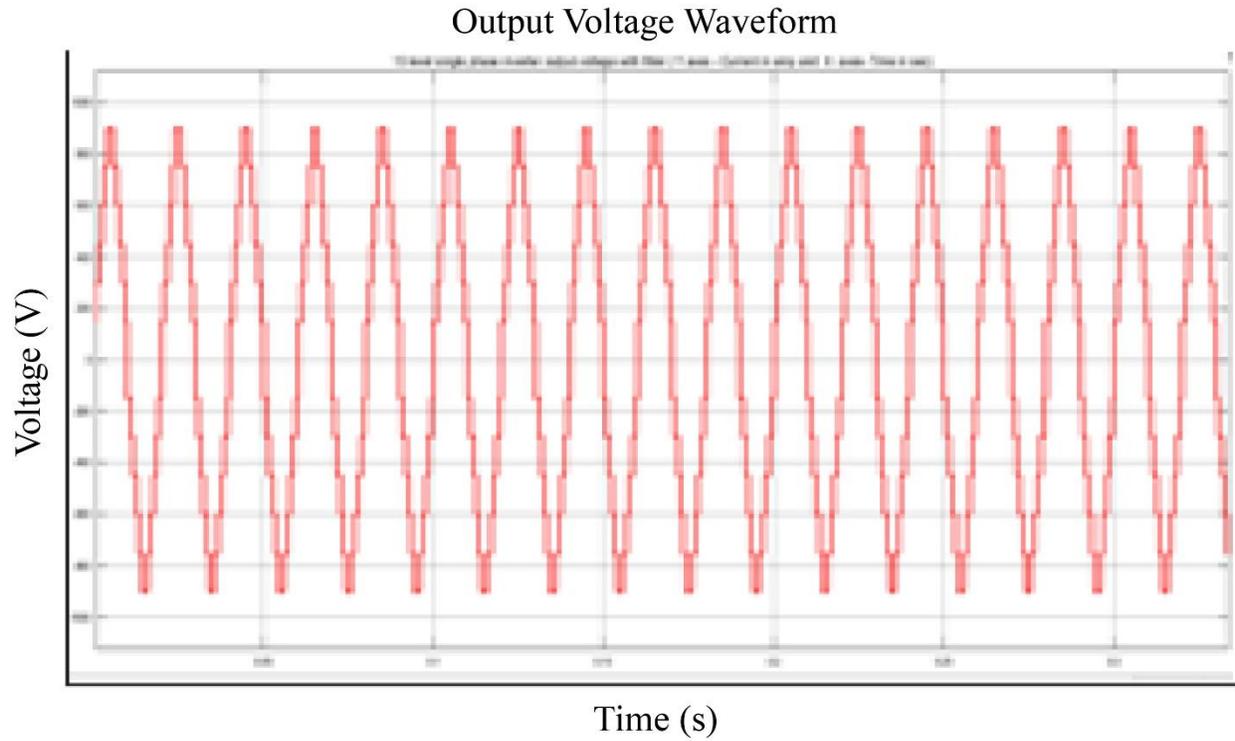


Fig. 7 An output voltage signal corresponding to the suggested 13-level innovative structure

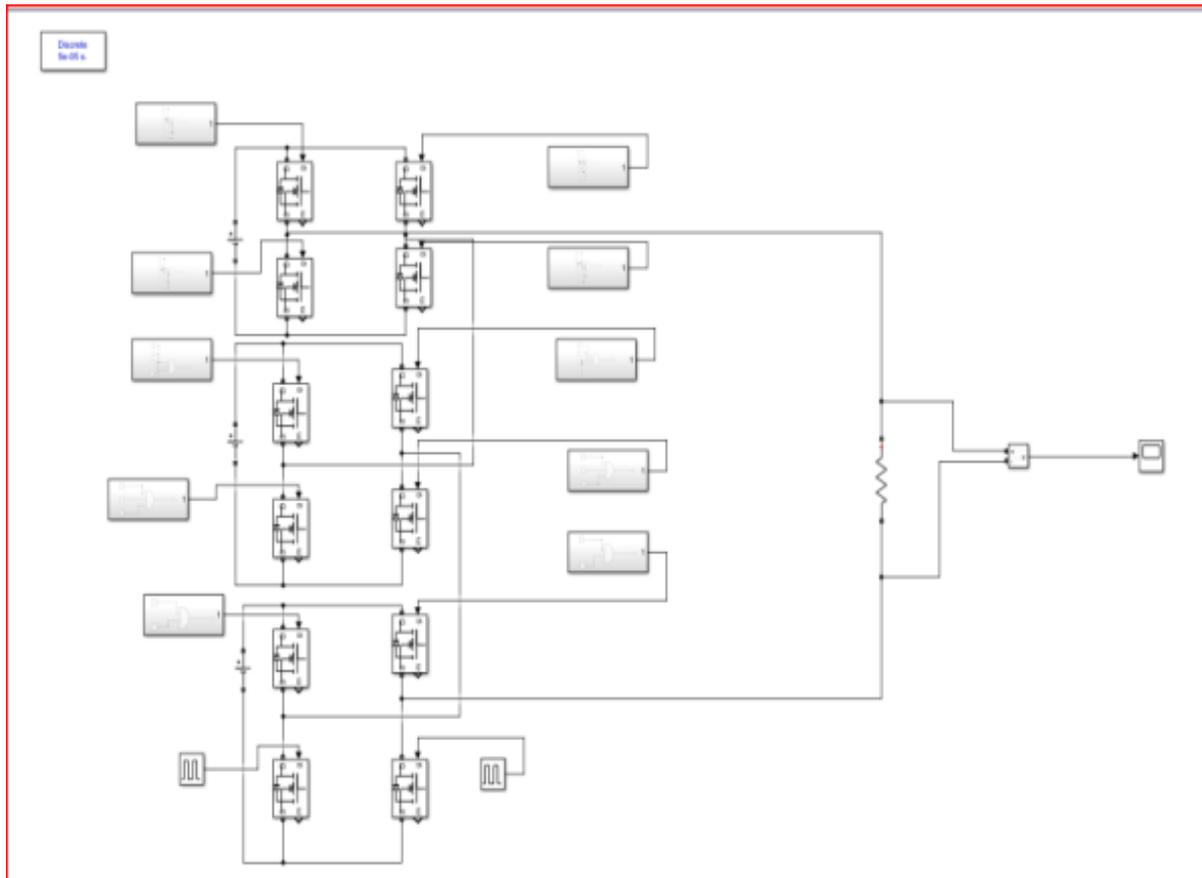


Fig. 8 Proposed 15-level novel cascaded topology's simulation diagram

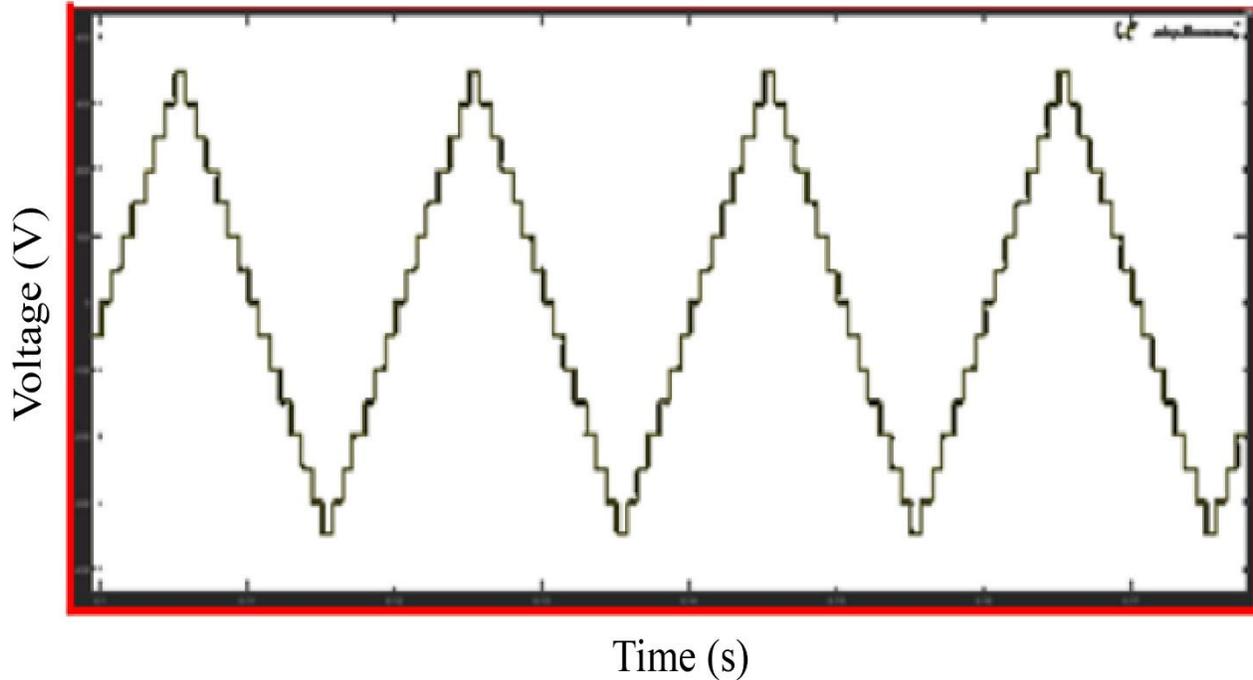


Fig. 9 Voltage waveform output for the recommended 15-level innovative topology

The suggested 13-level and 15-level CMLI Topology MATLAB/SIMULINK models were created to assess the efficiency, the output quality of the waveform, and Total Harmonic Distortion (THD). The simulation scenario included resistive-inductive loads, asymmetric DC sources, and a frequency of switching of 1 kHz with a modulation index of 0.9. The figures illustrate the simulation waveforms and FFT analysis for both inverter configurations.

For the 13-level inverter, the output waveform displayed well-defined stepped profiles, and FFT analysis indicated a THD of 8.08%. The 15-level inverter achieved a lower THD of 7.39% with increased resolution of the voltage steps. Efficiency is computed as

$$\eta = (P_{out} / P_{in}) \times 100.$$

The simulated efficiencies of the 13-level and 15-level systems exceeded 94%, confirming that the reduced-switch topologies did not compromise power performance. Switching loss analysis was also performed based on the switching transitions and current-voltage overlap. The use of LSPWM minimizes simultaneous high-voltage and high-current states, significantly reducing switching loss. Overall, the results confirm that the proposed inverter design achieves an acceptable waveform quality and harmonic suppression with far fewer switches, hence offering a small and effective solution appropriate for real-world applications in renewable energy systems and EV vehicles. Performance metrics such as THD, efficiency, switching loss, voltage stress, and component cost were analyzed and compared with conventional topologies.

4. Performance Analysis

4.1. Total Harmonic Distortion (THD)

From FFT results, THD is reduced significantly with more levels:

15-level MLI: 7.39%

13-level MLI: 8.08%

4.2. Efficiency Analysis

Efficiency (η) is evaluated as:

$$\eta = P_{out} / P_{in} \times 100$$

Where P_{out} is the load power, and P_{in} is the total DC input power. Simulation indicates:

15-Level: ~95.1%

13-Level: ~94.3%

4.3. Switching Losses

The total amount of switching operations per cycle was decreased by the reduced-switch topology. Estimated switching loss for each MOSFET

$$P_{sw} = 1/2 V_{ds} \cdot I_d \cdot t_{sw} \cdot f_{sw}$$

Cumulative losses dropped by 18–22% compared to conventional CHB with complete switch count.

4.4. Real-World Applicability

EV Drives: High-quality waveform reduces motor heating and torque ripple.

PV Applications: Low THD minimizes filter size and improves grid compliance.

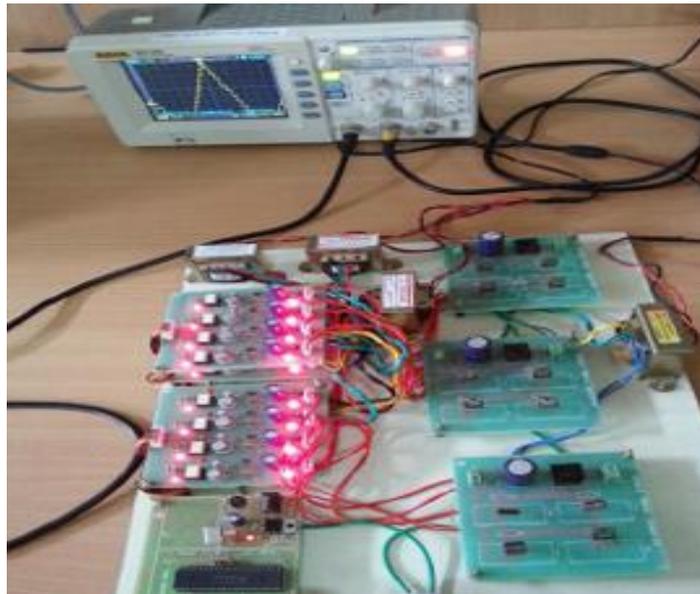
Table 1. Comparison of FFT analysis

S.No	Configuration	THD%	FFT ANALYSIS																						
1	5 Level New CHB MLI	31%	<p>FFT analysis</p> <p>Fundamental (50Hz) = 159.6, THD= 31.63%</p> <table border="1"> <caption>Approximate data for 5 Level New CHB MLI FFT</caption> <thead> <tr> <th>Frequency (Hz)</th> <th>Mag (% of Fundamental)</th> </tr> </thead> <tbody> <tr><td>50</td><td>20.5</td></tr> <tr><td>100</td><td>11</td></tr> <tr><td>150</td><td>19</td></tr> <tr><td>200</td><td>0.5</td></tr> <tr><td>250</td><td>4.5</td></tr> <tr><td>300</td><td>10</td></tr> <tr><td>350</td><td>18.5</td></tr> <tr><td>400</td><td>7</td></tr> </tbody> </table>	Frequency (Hz)	Mag (% of Fundamental)	50	20.5	100	11	150	19	200	0.5	250	4.5	300	10	350	18.5	400	7				
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2	7 Level New CHB MLI	16%	<p>FFT analysis</p> <p>Fundamental (50Hz) = 340.9, THD= 16.60%</p> <table border="1"> <caption>Approximate data for 7 Level New CHB MLI FFT</caption> <thead> <tr> <th>Frequency (Hz)</th> <th>Mag (% of Fundamental)</th> </tr> </thead> <tbody> <tr><td>50</td><td>10.5</td></tr> <tr><td>150</td><td>10</td></tr> <tr><td>250</td><td>0.8</td></tr> <tr><td>350</td><td>5.5</td></tr> <tr><td>450</td><td>1.8</td></tr> <tr><td>550</td><td>5.8</td></tr> <tr><td>650</td><td>1.2</td></tr> <tr><td>750</td><td>0.2</td></tr> <tr><td>850</td><td>5.2</td></tr> <tr><td>950</td><td>0.6</td></tr> </tbody> </table>	Frequency (Hz)	Mag (% of Fundamental)	50	10.5	150	10	250	0.8	350	5.5	450	1.8	550	5.8	650	1.2	750	0.2	850	5.2	950	0.6
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3	9 Level New CHB MLI	15%	<p>FFT analysis</p> <p>Fundamental (50Hz) = 302.7, THD 15.13%</p> <table border="1"> <caption>Approximate data for 9 Level New CHB MLI FFT</caption> <thead> <tr> <th>Frequency (Hz)</th> <th>Mag (% of Fundamental)</th> </tr> </thead> <tbody> <tr><td>50</td><td>8.2</td></tr> <tr><td>150</td><td>1.2</td></tr> <tr><td>250</td><td>3.2</td></tr> <tr><td>350</td><td>2.5</td></tr> <tr><td>450</td><td>0.4</td></tr> <tr><td>550</td><td>0.8</td></tr> <tr><td>650</td><td>2.8</td></tr> <tr><td>750</td><td>0.9</td></tr> <tr><td>850</td><td>4.7</td></tr> <tr><td>950</td><td>7.4</td></tr> </tbody> </table>	Frequency (Hz)	Mag (% of Fundamental)	50	8.2	150	1.2	250	3.2	350	2.5	450	0.4	550	0.8	650	2.8	750	0.9	850	4.7	950	7.4
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4	11 Level New CHB MLI	9.71%	<p>FFT analysis</p> <p>Fundamental (50Hz) = 396.6, THD= 9.71%</p> <table border="1"> <caption>Harmonic Magnitudes for 11 Level New CHB MLI</caption> <thead> <tr> <th>Frequency (Hz)</th> <th>Mag (% of Fundamental)</th> </tr> </thead> <tbody> <tr><td>50</td><td>5.5</td></tr> <tr><td>150</td><td>4.8</td></tr> <tr><td>250</td><td>2.5</td></tr> <tr><td>350</td><td>1.0</td></tr> <tr><td>450</td><td>2.6</td></tr> <tr><td>550</td><td>0.2</td></tr> <tr><td>650</td><td>1.8</td></tr> <tr><td>750</td><td>0.9</td></tr> <tr><td>850</td><td>0.6</td></tr> <tr><td>950</td><td>2.4</td></tr> </tbody> </table>	Frequency (Hz)	Mag (% of Fundamental)	50	5.5	150	4.8	250	2.5	350	1.0	450	2.6	550	0.2	650	1.8	750	0.9	850	0.6	950	2.4								
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6	15 Level New CHB MLI	7.39%	<p>Fundamental (50 Hz) = 283.1, THD= 7.39%</p> <table border="1"> <caption>Harmonic Magnitudes for 15 Level New CHB MLI</caption> <thead> <tr> <th>Frequency (Hz)</th> <th>Mag (% of Fundamental)</th> </tr> </thead> <tbody> <tr><td>50</td><td>0.018</td></tr> <tr><td>150</td><td>0.0175</td></tr> <tr><td>250</td><td>0.0175</td></tr> <tr><td>350</td><td>0.0175</td></tr> <tr><td>450</td><td>0.0175</td></tr> <tr><td>550</td><td>0.0175</td></tr> <tr><td>650</td><td>0.0175</td></tr> <tr><td>750</td><td>0.0175</td></tr> <tr><td>850</td><td>0.0175</td></tr> <tr><td>950</td><td>0.0175</td></tr> <tr><td>1050</td><td>0.0175</td></tr> <tr><td>1150</td><td>0.0175</td></tr> <tr><td>1250</td><td>0.0175</td></tr> <tr><td>1350</td><td>0.0175</td></tr> </tbody> </table>	Frequency (Hz)	Mag (% of Fundamental)	50	0.018	150	0.0175	250	0.0175	350	0.0175	450	0.0175	550	0.0175	650	0.0175	750	0.0175	850	0.0175	950	0.0175	1050	0.0175	1150	0.0175	1250	0.0175	1350	0.0175
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Table 2. Comparison with existing reduced-switch MLIs

Existing Work	Switch Count	DC Sources	THD (%)	Limitations
1)Siddique et al. (2019)	22 (13-level)	Multiple	12-14%	Large hardware, complexity
2)Babaei (2008)	18 (13-level)	Symmetric sources	13-15%	Balancing and voltage stress issues
3)Azib et al. (2023)	16+ (asymmetric EV topology)	Unequal	10-12%	High implementation cost
4)Lee et al. (2017) CCM-MLI	20+	Symmetric	10-11%	Heavily relies on complex PWM
5)Present Work (13-level)	10 switches	3 asymmetric sources	8.08%	—
6)Present Work (15-level)	12 switches	3 asymmetric sources	7.39%	—

**Fig. 10 Cascaded H bridge Fifteen-Level inverter experimental setup**

5. Experimental Set of A Fifteen-Level Inverter

The experimental architecture of the fifteen-level Cascaded H-Bridge inverter is depicted in Figure 10 below. The experimental results for the hardware are presented below. A comparison of FFT Analysis as illustrated in Table I.

6. Conclusion

The proposed 13- and 15-level novel CHB multilevel inverter topologies with reduced switches successfully achieved a lower harmonic distortion. The proposed novel 15- and 13-level cascaded multi-level inverter comprises three unequal voltage sources: DC sources, power diodes, and MOSFET design-powered switches. The switching losses were minimized using the proposed approach. The Total

Harmonic Distortion (THD) is further minimized. Based on the study above, it is evident that the suggested inverter is small, economical, and has reduced losses, all of which improve system efficiency. These attributes make it highly suitable for applications such as motor drives and low-power photovoltaic systems. Simulation results confirm their efficiency and applicability for medium-voltage, low-power systems such as EV drives and renewable energy converters.

6.1. Future Scope

Future work will therefore focus on (i) scaling the topology to three-phase operation and validating it under motor-drive conditions, (ii) examining the behaviour of the inverter under renewable sources and grid-connected environments.

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