Design and Implementation of 16-Bit Baugh-Wooley Multiplier

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Abstract

In this paper we centered upon the Design and Implementation of 16-bit Baugh-Wooley multiplier . Different electronic gadgets dependent on VLSI innovation have been important to the examination network from a very long while. These incorporate plans for adders and multipliers. This postulation focuses on a multiplication of marked number with two's complement shape, in particular the Baugh-Wooley multiplier and the device for this reason for existing was Xilinx ISE 14.2. The Baugh-Wooley multiplier with its fundamental writing survey and its Mathematical figuring for 16-bit multiplier was given reference to 4-bit engineering as in writing. It very well may be seen that the circuit comprises fundamentally of a few full-adders so a decent full-adder arrangement in Verilog-HDL straightforwardly adds to the productivity of the Baugh-Wooley multiplier. In this way the full-adder can be acknowledged in Xilinx ISE 14.2. At long last we plan in Xilinx and investigate the simulated result . The plan was observed to be proficient than the current structure of multiplier for two's complement numbers.

KEYWORDS *- Baugh-Wooley Multiplier ,Fulladder, VLSI, Xilinx.*

I. INTRODUCTION

Multipliers assume an imperative job in the present verilog programming and different applications. With advances in innovation, numerous analysts have attempted and are endeavoring to plan multipliers which offer both of the accompanying structure targets – fast, low power utilization, consistency of format and henceforth less territory or even blend of them in one multiplier along these lines making them reasonable for different rapid, low power and reduced VLSI implementation.The regular increase strategy is "include and move" calculation. In parallel multipliers number of halfway items to be included is the primary parameter that decides the execution of the multiplier. To diminish the quantity of incomplete items to be included, Modified Baugh-Wooley calculation is a standout amongst the most mainstream calculations. To accomplish speed enhancements Wallace Tree calculation can be utilized to decrease the quantity of consecutive including stages [1].

Further by consolidating both Modified Baugh-Wooley calculation and Wallace Tree method we can see favorable position of the two calculations in a single multiplier. Anyway with expanding parallelism, the measure of movements between the fractional items and middle of the road wholes to be included will build which may result in diminished speed, increment in silicon region because of anomaly of structure and furthermore expanded power utilization because of increment in interconnect coming about because of complex steering. A multiplier is one of the key equipment obstructs in most DSP frameworks. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis.

II. TYPES OF DIGITAL MULTIPLIERS

The multiplier architectures can be generally Classified into following categories:

- Serial multiplier
- Parallel multiplier
- Serial-parallel

A. Serial multiplier

The least troublesome method1 to perform increase is to incorporate arrangement of incomplete items. The successive multipliers use a dynamic development estimation. They are essential in structure in light of the fact that both the operands are entered consecutively. Hence, the physical circuit requires less equipment and a base proportion of chip area. In any case, the speed Performance of the consecutive multiplier is a result of the operands entered progressively.

B. Parallel multiplier

Most exceptional computerized frameworks join a parallel increase unit to complete rapid numerical tasks. A microchip requires multipliers in its arithmetic logic unit and an digital signal processing system requires multipliers to actualize calculations, for example, convolution and sifting. Parallel multipliers present fast execution, however are costly as far as silicon region and power utilization in light of the fact that in parallel multipliers both the operands are contribution to the multiplier in parallel way [2].
Some of these are

- Tree Multipliers
- Array Multipliers

C. Serial-parallel multiplier

In this the multiplier perceives the marked or unsigned 2"s supplement numbers and deliver them. the information y information is worked in parallel and bit sequential can be performed for augmentation. x information is feed over the multiplier for sequential activity. Then again, the sequential parallel multiplier is still multiple times quicker than a totally bit-sequential multiplier (which is generally extremely minimized), and less unpredictable to actualize than progressively refined calculations like for instance Booth multiplier.

III. BAUGH-WOOLEY MULTIPLIERS

The calculation which is having exhibit multiplication for two's supplement bits is Baugh and Wooley. The point of convergence of this multiplier is the sign bits of all the multiplicand and multiplier is unsigned or positive. This calculation is totally planned by utilizing the customary rationale full adders. Here twos supplement numbers multiplicated and after that at long last we get the items as (p0 – p6). The augmentation proposes of Baugh-Wooley Multiplier approach is spoken to underneath in fig1. Numerous ebb and flow DSP applications are gone for convenient, battery-worked frameworks, so control dissemination winds up one of the essential plan impediments With advances in innovation, numerous analysts have attempted and are endeavoring to structure multipliers which offer fast, low power utilization and consequently less territory in one multiplier along these lines making them reasonable for different rapid, low power and conservative usage. To accomplish speed enhancements Baugh Wooley Multiplication strategy utilized for marked augmentation. It isn't generally utilized a result of its multifaceted nature of its structure [3]. This paper inspects the quantity of LUT's utilized by the plan from accessible amount alongside the examination of IOB's and cuts for related and inconsequential rationale are finished.

This paper exhibits a calculation for parallel two's supplement duplication. The benefit of the calculation is the indication of all the halfway items bits are sure, which enable the item to be framed utilizing exhibit expansion system.

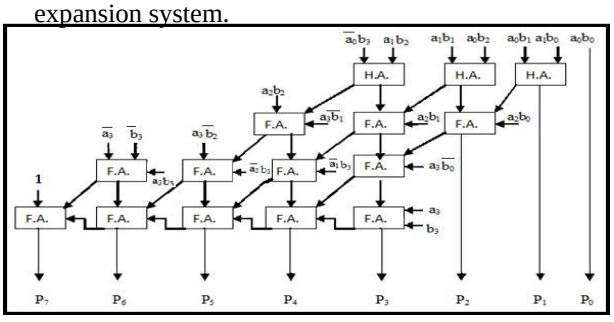


Fig1Architecture Of 4bit Baugh WooleyMultiplier

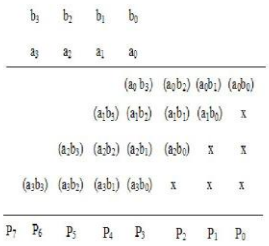
A. System Model Description

The exhibit multiplier Baugh-Wooley is an effective path for increasing both marked and unsigned numbers. Baugh Wooley calculation is utilized in High Performance Multiplier (HPM) tree, which acquires normal and rehashing structure of the exhibit multiplier.

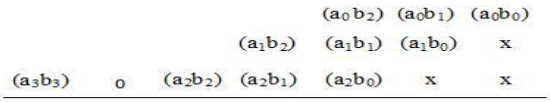
Baugh Wooley multiplier shows less postponement, low power scattering and the region possessed is likewise little contrasted with other cluster multipliers. The engineering of Baugh Wooley multiplier depends on carry savecalculation.

B. Working

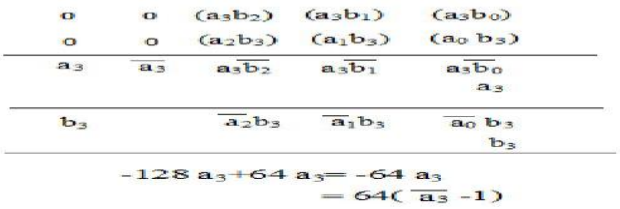
The multiplication algorithm can be represented as shown below. Here, two 4 bit numbers are multiplied using Baugh Wooley algorithm, and the partial products are given by Pp0 to Pp6 the MSB bits are signed bits and are represented using "bar".



addition of positive products



addition of negative products



$$-128\,a_3+64\,a_3 = -64\,a_3$$
$$= 64(\overline{a_3}-1)$$

Similarly

$$-128\,b_3+64\,b_3 = -64\,b_3$$
$$= 64(\overline{b_3}-1)$$

Therefore

$$64\,\overline{a_3} + 64\,\overline{b_3} - 128$$

Marked bits can be multiplicated utilizing this calculation, where all numbers are spoken to in their 2's supplement frame for this the design is somewhat altered by including a XOR door, the info is first given to the XOR gate, consequently changing over the number to its 2's supplement form[4]. The XOR gate has the multiplicand as one information and a

control line which is associated with an empower as another information.

At the point when the empower line goes high the XOR doors transform the information add a 1 to the bits bringing about the 2's supplement of the number. At the point when the empower line is low the bit is passed accordingly with no reversal.

C. Objectives of Baugh Wooley Multiplier

- Understand the Baugh-Wooley increase calculation for 2's compliment information.
- Design the 2's compliment multiplier dependent on carrysave
- Employ hierarchical design techniques.
- Simulate the multiplier performance.
- It presents an efficient implementation of delay, bonded IOB'S, no. of slices and no of LUT of Baugh Wooley Multiplier.

D. Baugh Wooley Multiplier Evaluation

The fractional item age in the Baugh-Wooley (BW) execution is a lot less difficult than the one utilized in the adjusted Booth multipliers. This distinction in unpredictability winds up obvious likewise when we manage fan out. In the BW multiplier each information drives N 2-information AND-doors for a N-bit multiplier.

The push to drive the AND-gates can just be shared between a quantities of inverters that interface with the multiplier essential information sources. Baugh-Wooley Multiplier is utilized for both unsigned and signed number multiplication. Signed Number operands which are spoken to in 2's complemented shape. Partial Products are balanced with the end goal that negative sign move to last advance, which thusly expand the normality of the multiplication array . Baugh-Wooley Multiplier works on marked operands with 2's complement portrayal to ensure that the indications of every single incomplete item are sure. The outcomes demonstrate that the Baugh-Wooley multiplierhas expanded speed since clock period isonly15.861ns. Pipeline organizes further enhance theBaugh - Wooley architecture speed. Number of LUTs speaks to the area required for implementation.The number of LUT required in Baugh-Wooley design is 30 contrasted with 32. The fan-out of the multiplier design is additionally given which straightforwardly gives the likelihood of the multiplier to large circuits[5]. This can be stretched out to the pipelined multiplier engineering additionally to confirm the parameters. Inactivity and speed are the critical elements with pipelining under thought. The blend consequences of 4-bit pipelined multipliers are appeared Table 2.Power utilization in Baugh-Wooley multipliers is least contrasted with other traditional multiplier units. So it clears that the marked parallel increase through Baugh-Wooley augmentation is suited for extensive multiplier execution. The upgrades in limitation can be utilized to make Baugh-Wooley multiplier increasingly proficient. The fan-out of the multiplier structures are likewise given which specifically gives the likelihood of the multiplier to shape expansive circuits. This can be stretched out to the pipelined multiplier design additionally to check the parameters. Dormancy and speed are the vital elements with pipelining under thought. The blend aftereffects of 4-bitpipelined multipliers are appeared Table 2. The pipeline requirement builds the speed of the multiplier significantly with an expansion in power utilization. For the Baugh-Wooley multipliers,the clock period decreases to 3.321ns because of pipe line registers executed [6].

This enhances the speed which may diminish because of the BK adder which I utilized in my engineering. The most extreme deferral for this design is 2.143ns.i am utilizing 65 Flip Flop out of 17088 and greatest recurrence is 527.037MHZ which is a decent sign .The fuse of the pipeline multipliers hence can be successfully done to make the chip effectively reconfigurable among the two reconfiguration modes and this work is in progress[7]. The likelihood of other reconfiguration requirements is under work and the usage of the reconfiguration modes as indicated by these limitations are the future work.

IV. RESULTS

A. Results of 4 bit Baugh Wooley Multiplier

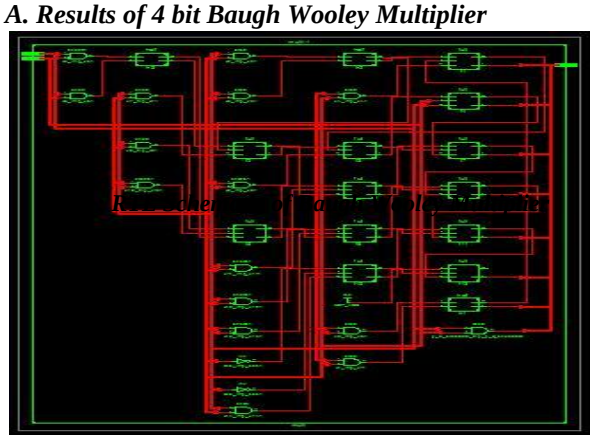


Fig.2 : RTL Schematic of Baugh Wooley Multiplier

Fig.3 : Simulation Results

B. 8-bit Baugh Wooley Multiplier

The code for multiplier is written in Verilog dialect. The RTL Compiler is utilized to aggregate

the code. The Encounter (rhythm) programming is utilized for floor arranging, control arranging and directing reason. The usefulness of the schematic is confirmed utilizing Virtuoso programming. The significant piece of the structure passage was done at the transistor schematic dimension. The design where done with sights set on evaluating the region of the multiplier. Structures were entered utilizing Cadence RTL compiler, utilizing Encounter floor-arranging, control arranging and steering is completed.

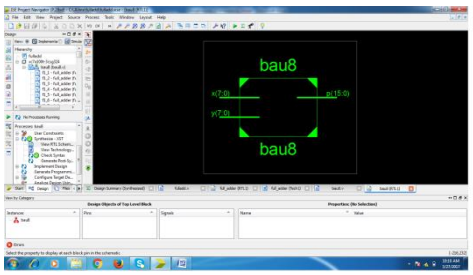


Fig.4 : 8-bit Baugh Wooley RTL Schematic Simulation

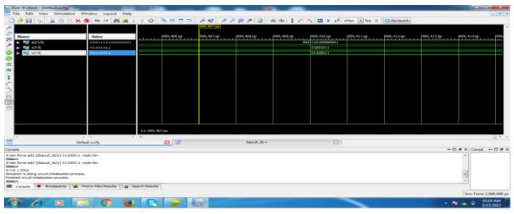


Fig.5 : 8-bit Baugh Wooley Multiplier Results

C. 16-bit Baugh Wooley Multiplier

Baugh-Wooley multiplier which were having extremely huge applications in DSP processors, flag and frameworks where convolution of flag is required. The creators in different papers demonstrates a cross way to deal with framework structure, through dealings among the calculation plan and center engineering and circuit achievement, can surrender the most noteworthy up degree in structure multifaceted design. In this work has been appearing by the Verilog execution for framework configuration to get the consequences of different numerical ideas. The GDI based structuring of the multiplier at different CMOS innovation level gives different aftereffect of enhancement in the field of multifaceted nature decrease. The streamlining of transistor or MOS chips is the significant worry in the developing innovation in the structure of different multiplier engineering with connected calculations [8].intricacy. In this work has been showing by the Verilog implementation for system design to obtain the results of various mathematical concepts. The GDI based designing of the multiplier at various CMOS technology level gives various result of improvement in the field of complexity reduction. The optimization of transistor or MOS chips is the major concern in the growing technology in the design of various multiplier architecture with applied algorithms [8].

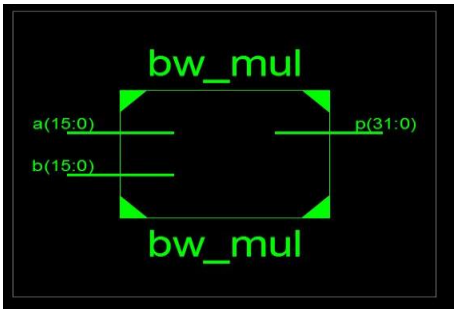


Fig.6 : Schematic of 16x16 Bit Baugh-Wooley Multiplier

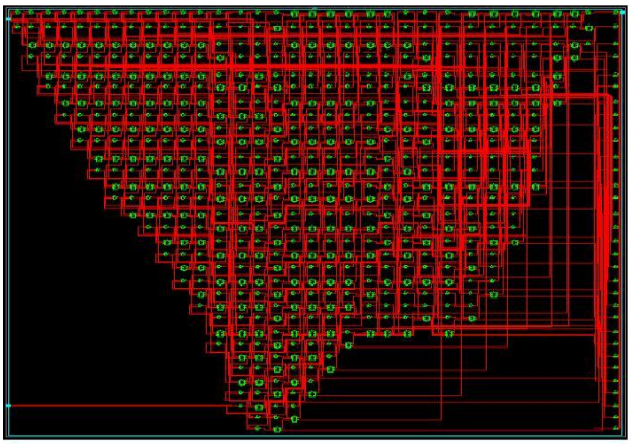


Fig.7 : Output Waveform For Some Random Number Taken In Test Bench

V.CONCLUSION

A 16-bit marked multiplier was configuration utilizing programming Xilinx of adaptation 14.2 .By utilizing this multiplier the deferral is less when contrasted with different multipliers. And in addition Baugh Wooley expends less power when contrasted with ordinary Booth Multiplier. Power can be further lessen by actualizing the structure utilizing most recent innovation i.e, Modified Baugh Wooley Multiplier.[9]

There is gigantic extension in structure of multiplier in various models. The Baugh Wooley is utilized for 2's complement marked augmentation. There are different designs for 2's supplement marked increases. The equivalent can be actualized utilizing

most recent innovation hub, for example, Modified Baugh Wooley Multiplier.[10]

This paper shows a basic and profoundly effective strategy for augmentation fundamentally utilizing 2's supplement it is a technique for various leveled multiplier plan which unmistakably demonstrates the computational favorable circumstances offered by the convey spare snake. The postponement for 16x16 piece Baugh-wooley multiplier is 8.25 ns and no of LUT's are 30 and fan-out is 46 . It is seen that baugh-wooley multiplier is quicker in execution when contrasted with other ordinary multiplier and consequently suited for reconfiguration.

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